

# EDA Trends You Can't Ignore

## How Short Product Cycles Are Stirring the EDA Industry

Sponsored by:

**EDA**

CONSORTIUM

Emerging Companies  
Committee



**Silicon Valley Bank**

&

**D^Side Advisors**

# Organizers

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- **Steve Pollock, Chairman of the EDAC Emerging Companies Committee**
- **Charles DiLisio, President, D-Side Advisors**
- **Jim Hori, Vice President, Silicon Valley Bank**
- **EDAC staff**

# EDA Customer Trends

- **Redefining design investment in software vs. hardware tools**
- **Leveraging open source software to reduce product development cost**
- **Reducing EDA tool integration costs through tool interoperability**
- **Changing EDA valuations, both venture and acquisition**

# Panel

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- **Greg Spirakis**  
VP, Technology & Manufacturing Group and  
Director of Design Technology (DT), Intel
- **Robert Payne**  
SVP and GM, Philips Semiconductor
- **Kevin Morgan**  
Vice President, Engineering, MontaVista
- **Charles Welch**  
Managing Director, SVB Alliant

# **Emerging Consumer Market — Trends You Can't Ignore!**

by  
Charles DiLisio  
**D·Side Advisors**

September 22, 2004

**[cdilisio@dside.com](mailto:cdilisio@dside.com)**

# Consumer-Like Markets — Changes The Playing Field!



## IC Design Issues:

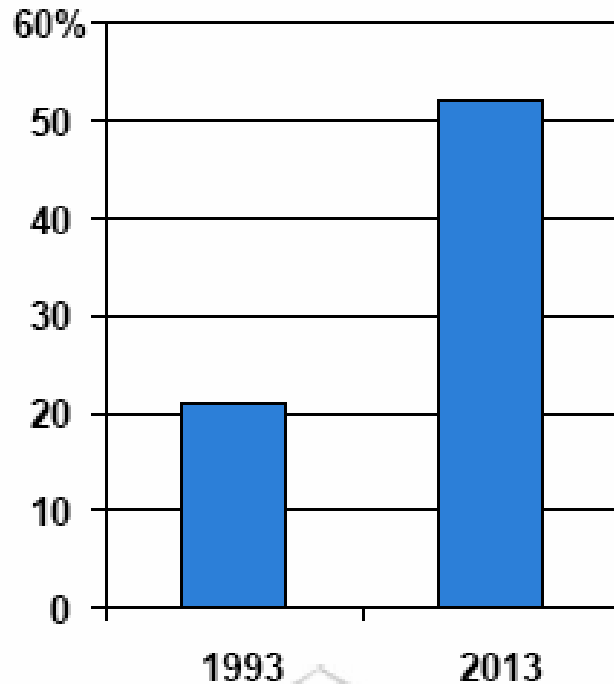
- Feature Set
- Technology Mix
- Volume (moderate)
- Time to Market
- Edsel vs. Mustang

All at a ....

## Non-Spousal Approval Price Point

# Consumer Markets Drive IC's

Consumer percent of semiconductor market



Gartner Dataquest  
Semiconductor Industry Summit

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## CE Pose Design Challenge

- Non-Spousal Approval Price Point vs. Corporate Sign-Off
- Al Dente Marketing vs. Planned, Defined Markets
- Highly Segmented Markets vs. Big, Deep, Markets
- Silicon Platforms vs. Accelerating ASIC Cost

# Semiconductor Industry's Fundamental Model... **Is BROKEN!**

**Non-Spousal  
Approval Price**

**In-elastic Demand  
Highly Segmented**

**Silicon Integration  
Design Cost  
\$15-\$25M/design**

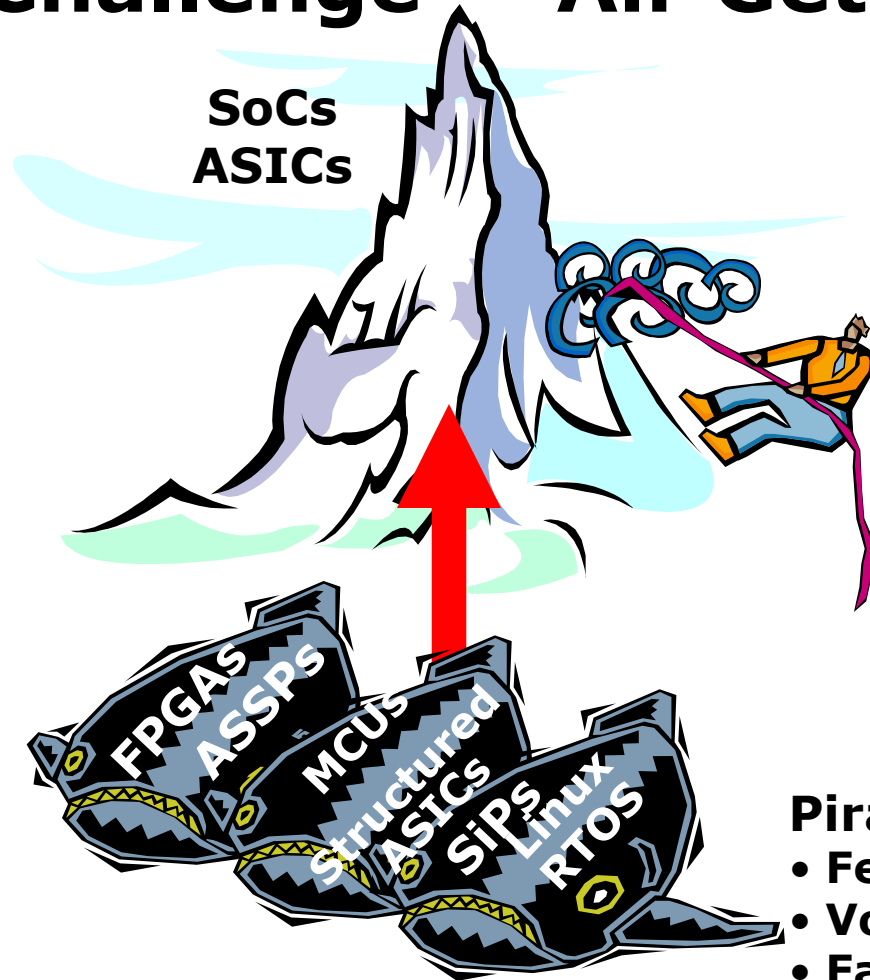
**Silicon "Shrinks"  
Now Costly!**



# Everest Challenge — Air Gets Thinner!

**Valued  
by  
IC  
Design**

**Valued  
by  
Systems  
Vendor**



**Piranha Provide**

- Feature Flexibility
- Volume Flexibility
- Faster Time to Market
- Lower Cost

# Be the Rugged Individualists in EDA

- ♦ Tool Interoperability
  - Allows emerging companies to innovate
  - IC design groups get best of breed
- ♦ Platform ICs
  - Platform ICs (ASSPs, structured ASICs) provide performance and cost advantage
  - EDA vendors support hardware and systems design
- ♦ Embedded Software
  - System design flexibility over hardware
  - Time to market advantage

# Pepper . . . and Salt

THE WALL STREET JOURNAL



“At this point maybe we’re just not ready to commit to a Wi-Fi enabled Linux-based pasta machine.”

**Think!**

**Value**

**Growth**

**Profit**

**Charles DiLisio**  
**[cdilisio@dside.com](mailto:cdilisio@dside.com)**

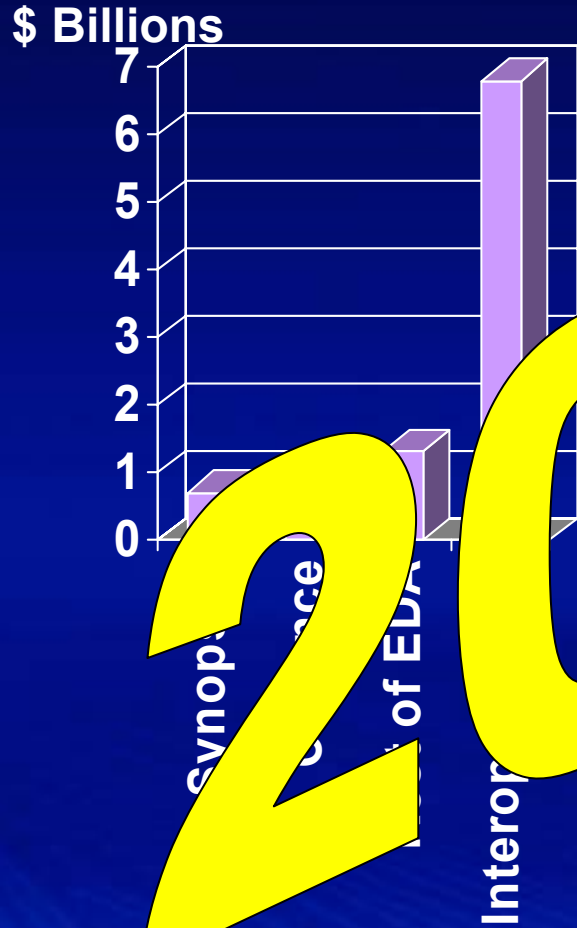
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- ♦ **Bob Payne**, Senior VP/GM Advanced System Technology — Philips Semiconductors
- ♦ **Kevin Morgan**, VP Engineering — MontaVista Software
- ♦ **Charles Welch**, Managing Director — SVB Alliant

**Greg Spirakis**  
**Vice President, Technology & Manufacturing Group**  
**Director, Design Technology**

**September 22, 2004**

# Interoperability is Expensive!!



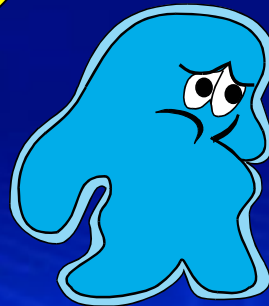
2000

“We spend \$3-5 on interoperability for every \$1 spent on EDA tools”

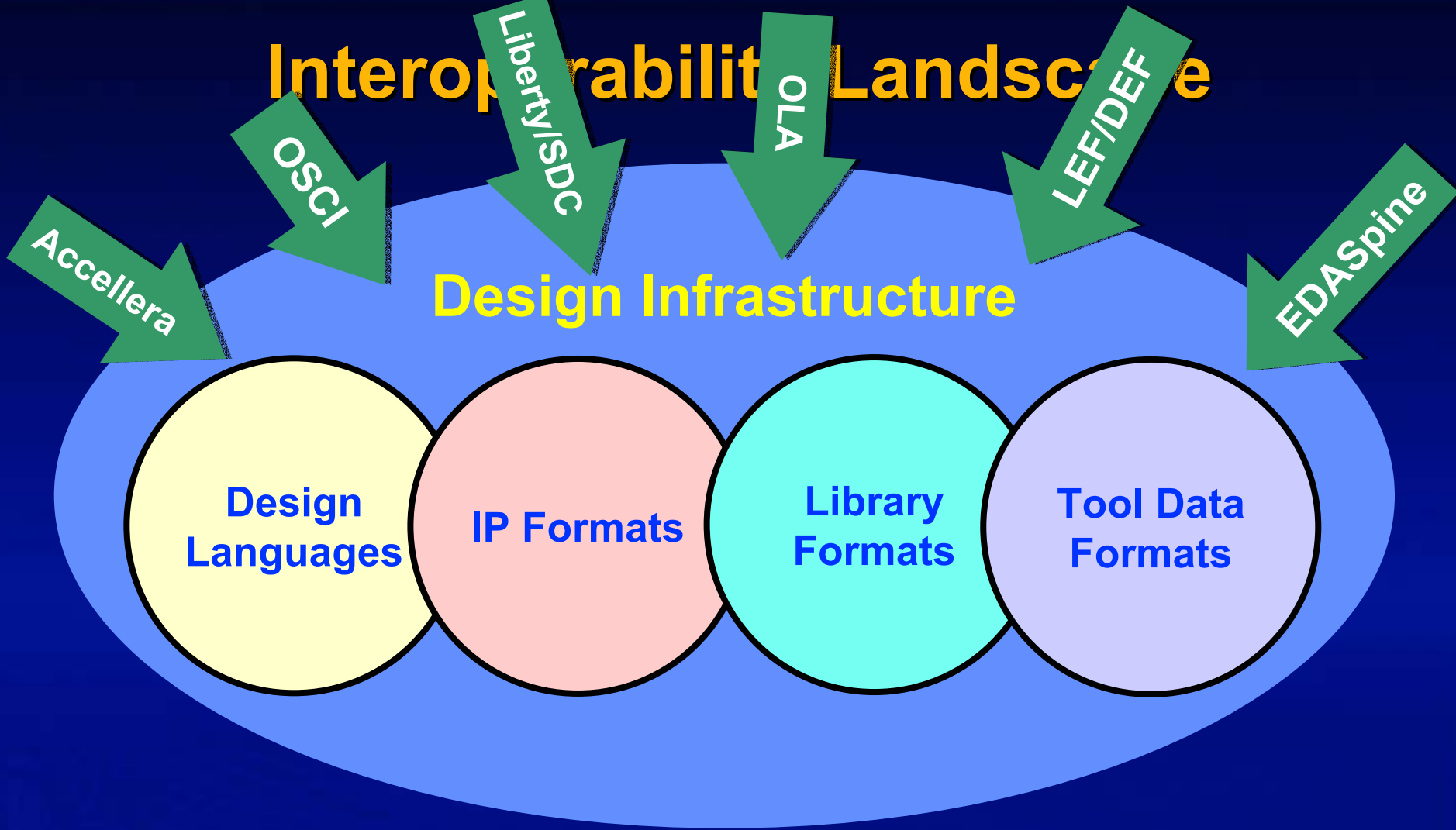
Gadlinger, Intel

“The industry is spending \$7-9 billion a year on interoperability work together”

- Ron Collett, Collett International



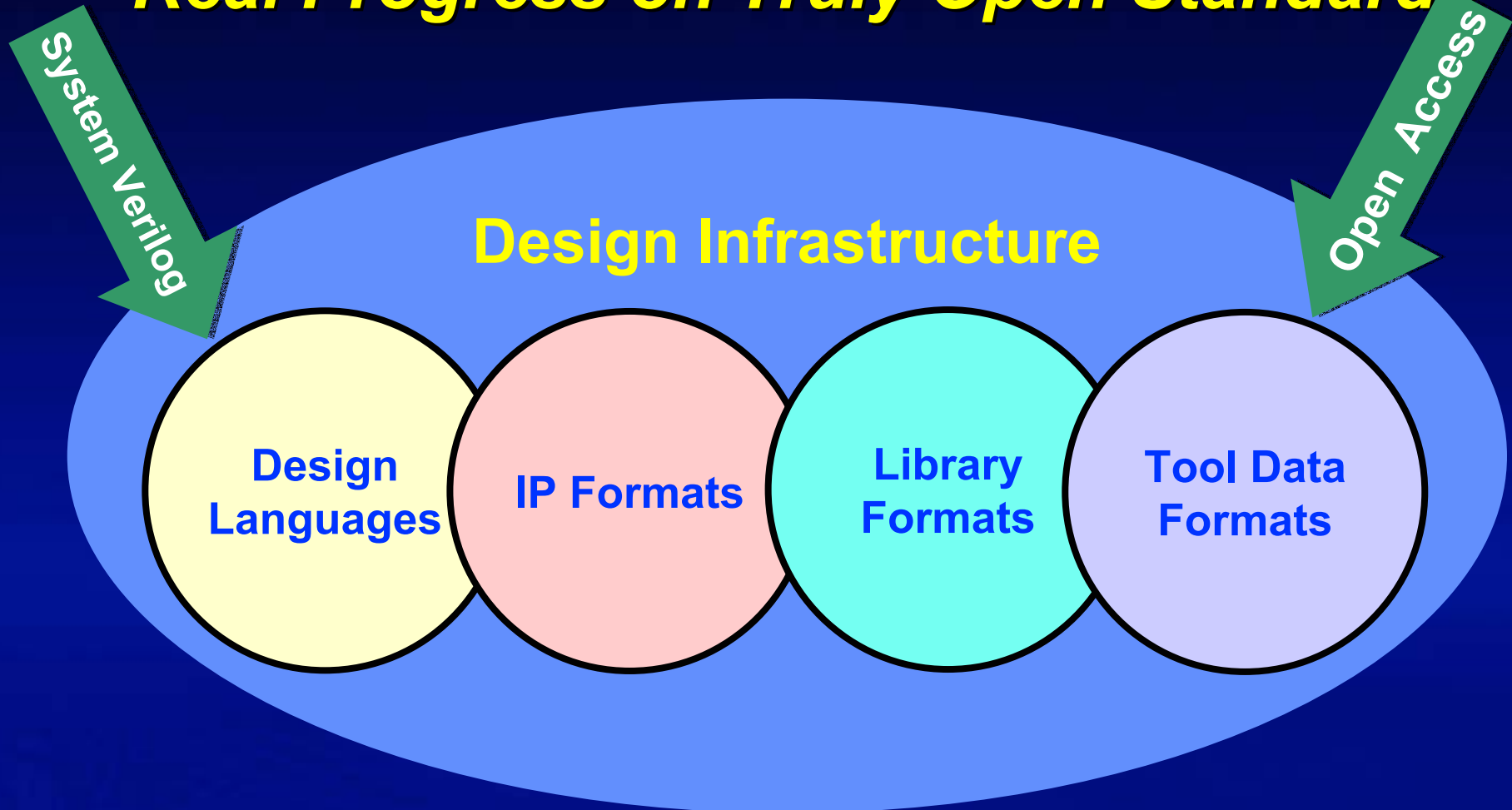
# Interoperability Landscape



***Lots of Activity !!!***

**DAC 2000 Interoperability Workshop**

# Real Progress on Truly Open Standards



- SystemVerilog Is THE Verilog Of The Future
  - IEEE Standard Efforts Unified
- OpenAccess Has Reached Critical Mass
  - 28 Members, Version 2 Released, Community Contributions

# What Did We Learn

- Standards Efforts Can Work In EDA IFF
  - Solves A Real Problem
  - Customer Driven
  - Truly Open
- InterOp Costs Dropped From 3:1 To 1:3\*
  - Probably Over Estimated Initially
  - API Driven Tools Truly Easier To Integrate
  - One Time Costs Already Absorbed
- Arriving Late To The Party Hurts
  - Companies Joining SystemVerilog Bandwagon Late Are At Competitive Disadvantage
- Technology Need (Vs Cost) Will Drive Future Standards
  - Extend OpenAccess To Masking/Manufacturing
  - Customer Driven Open Library Standard

▪ <http://www.si2.org/Projects/lcc.html>

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# PHILIPS

Panel Discussion:  
How Short Product Life Cycles are  
Stirring the EDA Industry?  
“Trends You Can’t Ignore”

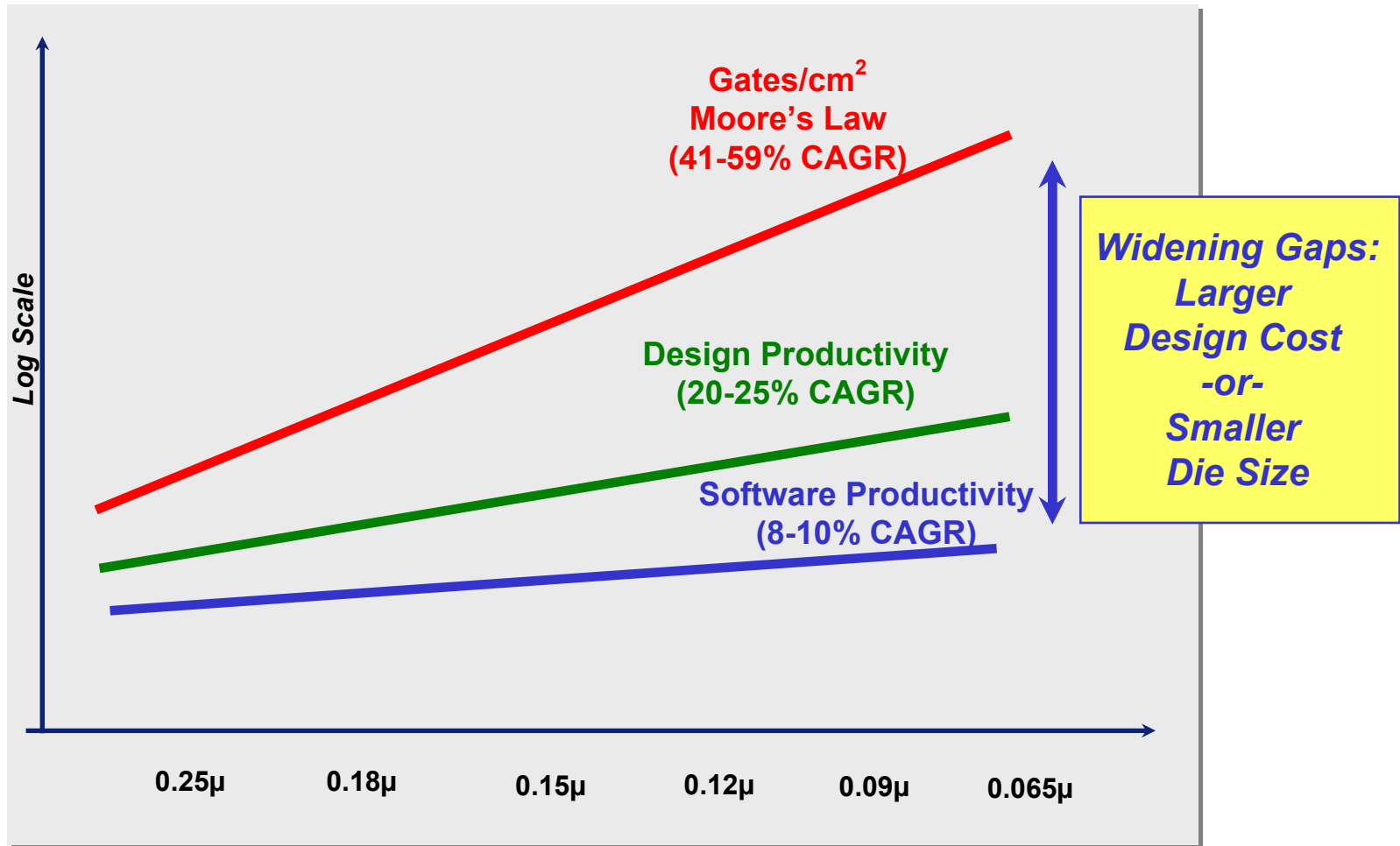
Bob Payne

SVP/GM Advanced Systems Technology

Philips Semiconductors CTO Organization

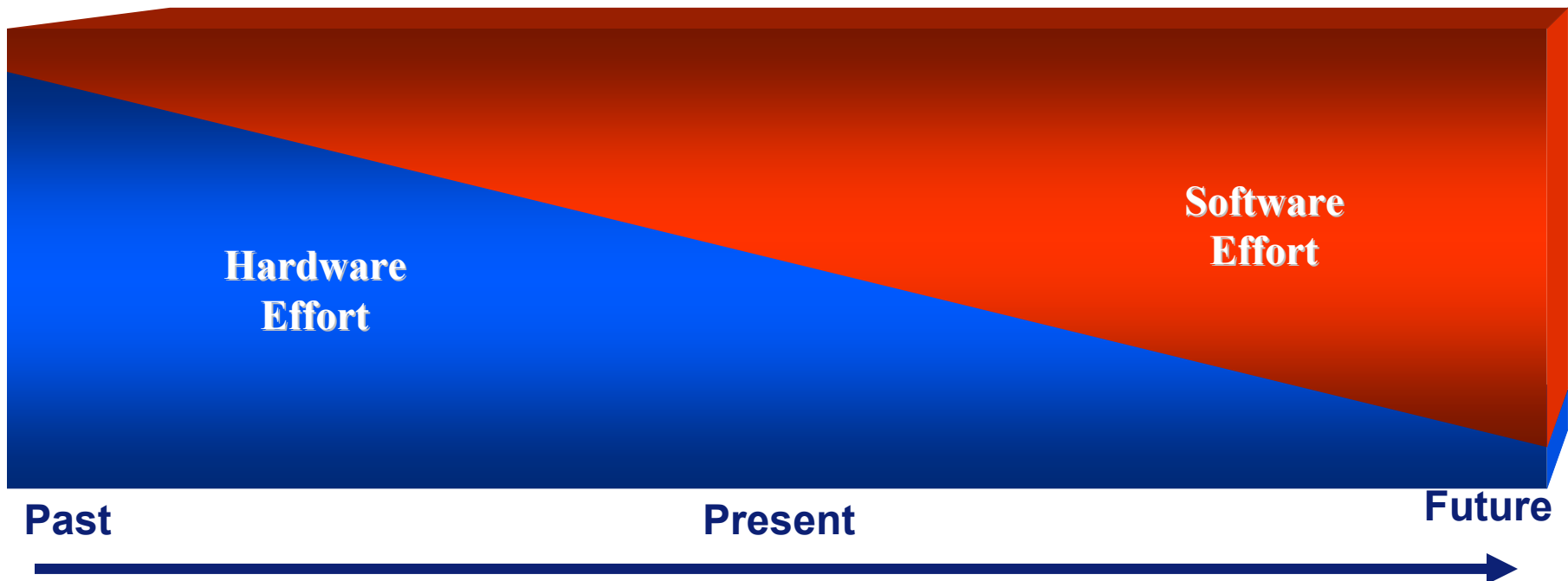
Sept. 22<sup>nd</sup>, 2004

# Design Productivity Gap



# Why the Software Productivity Concern??

- In the end; if we solve the HW design productivity and fail to address the SW productivity we have accomplished little.
- **System design productivity** is the objective.



# The Trends:

- Productivity shortfall manifesting itself as an increasing average design cost from generation to generation – Probably doubling every four years (\$10M and Growing)
- Targeted production revenue needs to be 10X the development since system R&D spending is generally held to 10% of revenue
- Fewer sockets can produce the targeted revenue and therefore we see fewer design starts
- More SW programmability/re-configurability is required to cast a bigger production revenue shadow and address time to market

# SOC Key Issues

## Correct Functionality

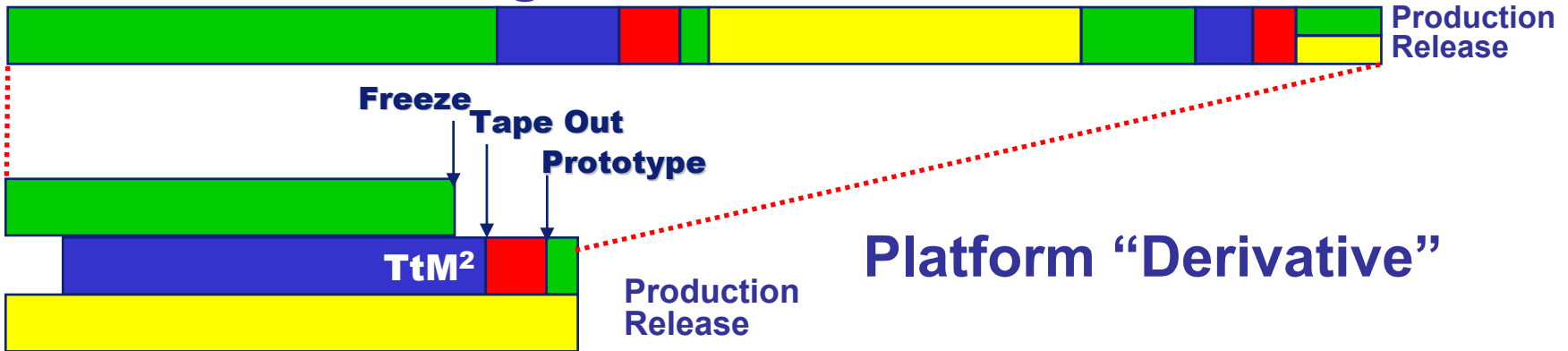
Cycle Rate	Debug (Hrs)	Debug Time	Technology		
1	1	1 Hour	Silicon Reference Design	Simulation	Hardware
$10^{-1}$	10	~1 Working Day	FPGA		
$10^{-2}$	100	4 Days	HW Emulator		
$10^{-3}$	1,000	1.4 Months	Throughput Model	Simulation	Software
$10^{-4}$	10,000	1.2 Years	Transaction Model		
$10^{-5}$	100,000	~12 Years	Cycle Accurate Sim Model		
$10^{-6}$	1,000,000	>1 Lifetime	RTL Model		
$10^{-7}$	10,000,000	~1 Millenium	Gate Level Model		

Hours of Testing Experience are Required

A Reference Design is the Least Abstract & Most Accelerated

# Platform “Derivative” Design

## Conventional Design Process



- **Hardware Software Co-Design**
- **Physical Co-Design**
  - Change Friendly Design Process
  - Timing Closure Friendly Architecture
  - Handoff Friendly Methodology

# Evolution of SoC Enemy #1

- When I started to design ICs **PERFORMANCE** was my biggest concern.
- As I matured into management **COST/DENSITY** was my biggest concern.
- Now **POWER** has emerged as my biggest concern.
  - Why?
  - Interesting Observations About Designing For Low Power!

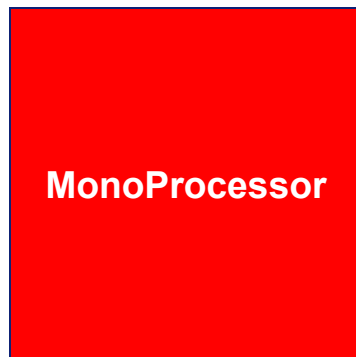
# Some Shocking Observations!

- **How much Power would a Performance Focused IC Consume?**
  - 3GHz Pentium 4 runs  $>75W = 50A * 1.5V$
  - Only about 10% of the chip runs at 3GHz
  - If the entire chip were run at the Compute Engine speed the chip would consume  $> 500W/square\ cm$
  - Extrapolation of this trend indicates future technology will exceed  $1KW/square\ cm$ .
    - I am told that this is same power density as nuclear reactor
- **Practical Limits:**
  - Consumer Electronics  $\Rightarrow 2.0W\ to\ 4.0W$
  - Mobile Electronics  $\Rightarrow 0.2W\ to\ 0.4W$

## Which Wish Should Be Granted?

Wish #1

World's Fastest  
"Do All"  
MonoProcessor



Wish #2

Simple Control  
Processor and "Farm"  
of Streaming Engines



# Orchestra Analogy

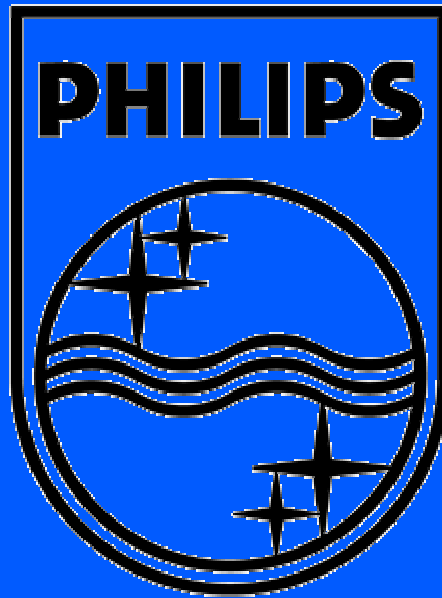
**RISC Processor = Conductor**

**Streaming Processors = Musicians**

**Information Pipes = Patrons**



- **Best Computation Per Square Millimeter**
- **Best MediaStones Per Mille-watt**
- **Turning into industry trend**



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A large blue banner with rounded corners containing the title text. The background of the banner features a faint world map and a stylized architectural structure with perspective lines.

# Linux Technology in New System Architectures

**Kevin Morgan**  
**Vice President,**  
**Engineering**  
**September 22,**  
**2004**

Shift to MMU-full 32 bit microprocessors as the “host controller” in system designs.

Increasing memory density and increasing peripheral capability reducing “super-fast” real-time demands on the host processor and host OS.

Trend toward “intelligent connected everything”. All product categories are enhanced by (1) embedded intelligence and (2) internet connectivity.

The technology recession and hyper-competition driving the need for cost savings: “do it yourself” OS’s (traditionally a giant segment of the market) are history.

The spread of Unix as a standard common computing and development platform.

The disruptive values of open source!!

Linux/GNU software is ***DISRUPTIVE TECHNOLOGY*** for embedded systems.

New/unique values brought to bear as a result of open source nature combined with embedded market requirements:

- ◆ Ease of customization of all level of system software.
- ◆ Availability of development talent worldwide.
- ◆ Availability of enabling software for leading h/w technology.
- ◆ Vendor independence.

Traditional vectors of competition over-satisfied by traditional solutions:

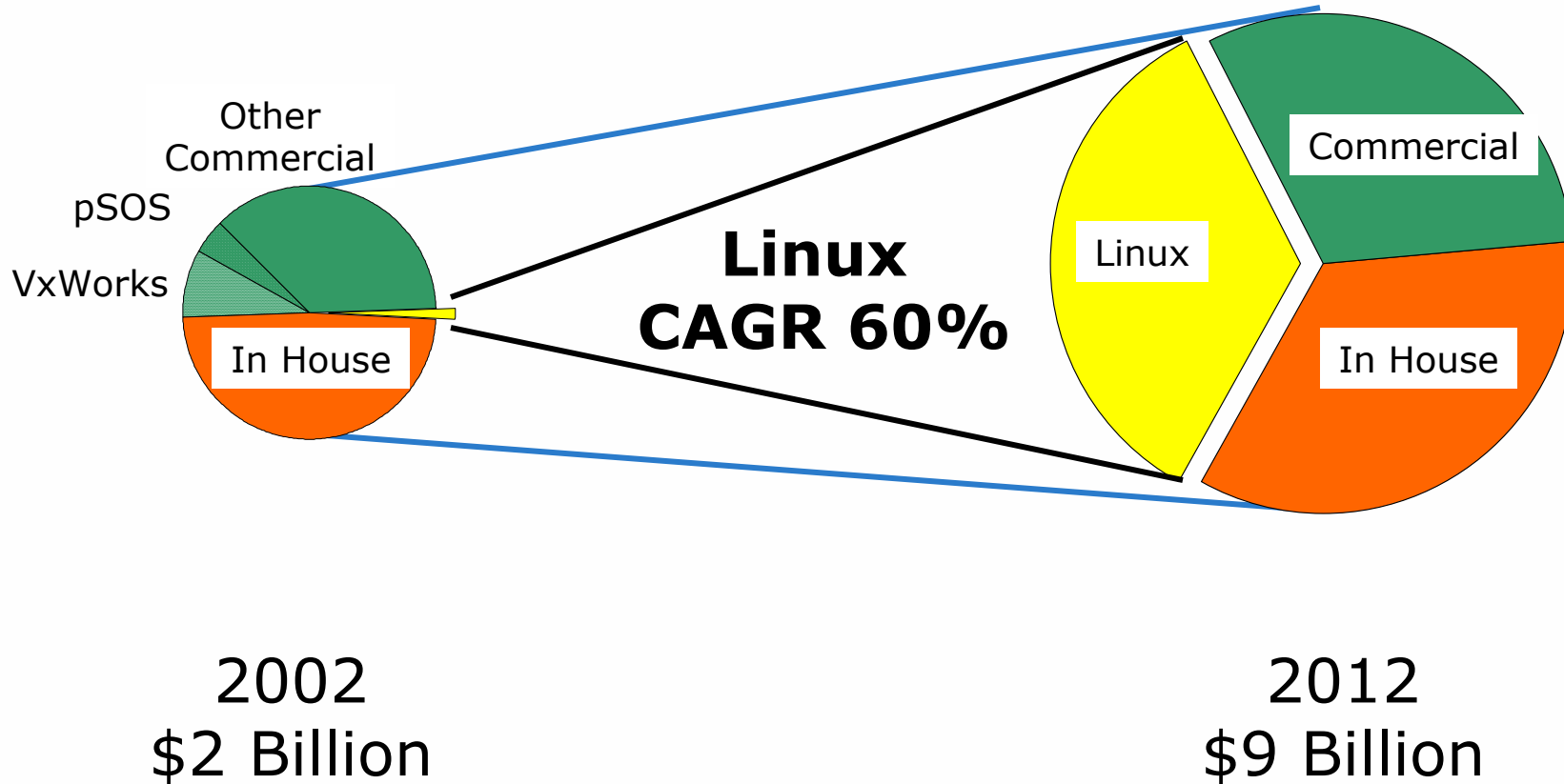
- ◆ Real-time response
- ◆ Footprint

New product categories and underlying technology evolution reduces the need for extreme capabilities in these two areas.

We have shifted into the early majority phase of the embedded Linux market:

- ◆ 1999-2001: early adopters
  - ❖ Open acknowledgement of lacks, “I want to use it anyway”
- ◆ 2001-2002: “the chasm”
  - ❖ “Tell me about who else in my industry is using this?”  
Answer: you are the first!
- ◆ 2003-??: early majority
  - ❖ “My competitors have Linux based offerings and my customers are asking me where’s mine...”

# The Hot Growth in Embedded is in Linux



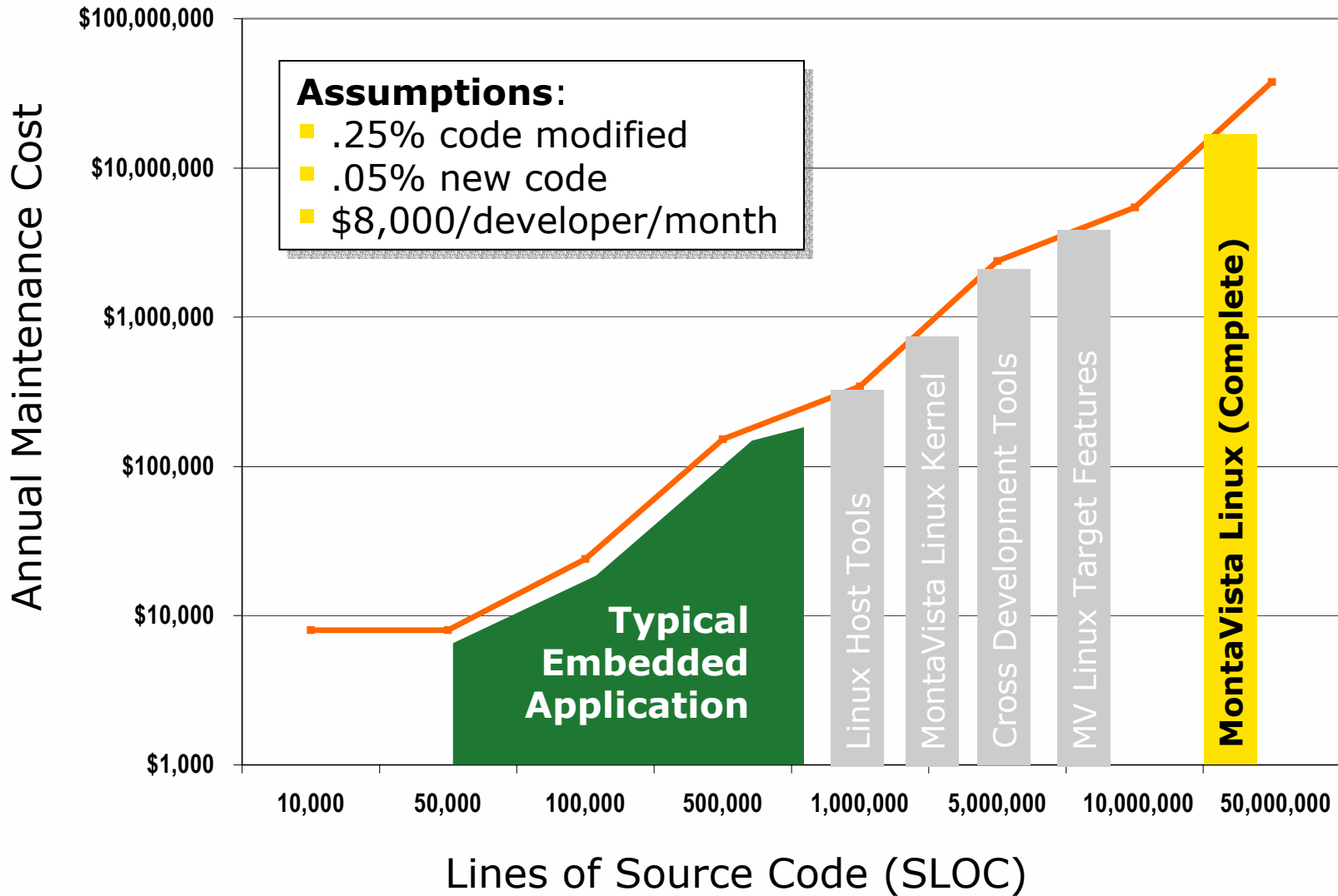
Source: Company & VDC data

# The Role of Commercial Linux Vendors for Product Developers

Do-it-yourself approaches to crafting open source based embedded solution software is viable BUT...

- ◆ Cost is always a function of content/size.
- ◆ Vacuuming the web is just the START of your software cost equation, not the end!!
- ◆ The more you vacuum, the larger your steaming pile of technology becomes, with all that that implies.
- ◆ Value addition to meet specific requirements...integration...testing...packaging...support...all the traditional “proprietary” issues and values are still extremely important to users! And no less expensive to deal with...
- ◆ ...particularly when you reach the point of vacuuming literally 10's of millions of LOC!!
- ◆ The role and the value provision of vendor solutions quickly becomes apparent to those who understand software economics.

# Investment to Create and Maintain Linux-based Embedded Platform



Linux is the single most significant threat to Microsoft today, and arguably ever.

Anti-Microsoft sentiment is high world-wide, and Linux is the alternative.

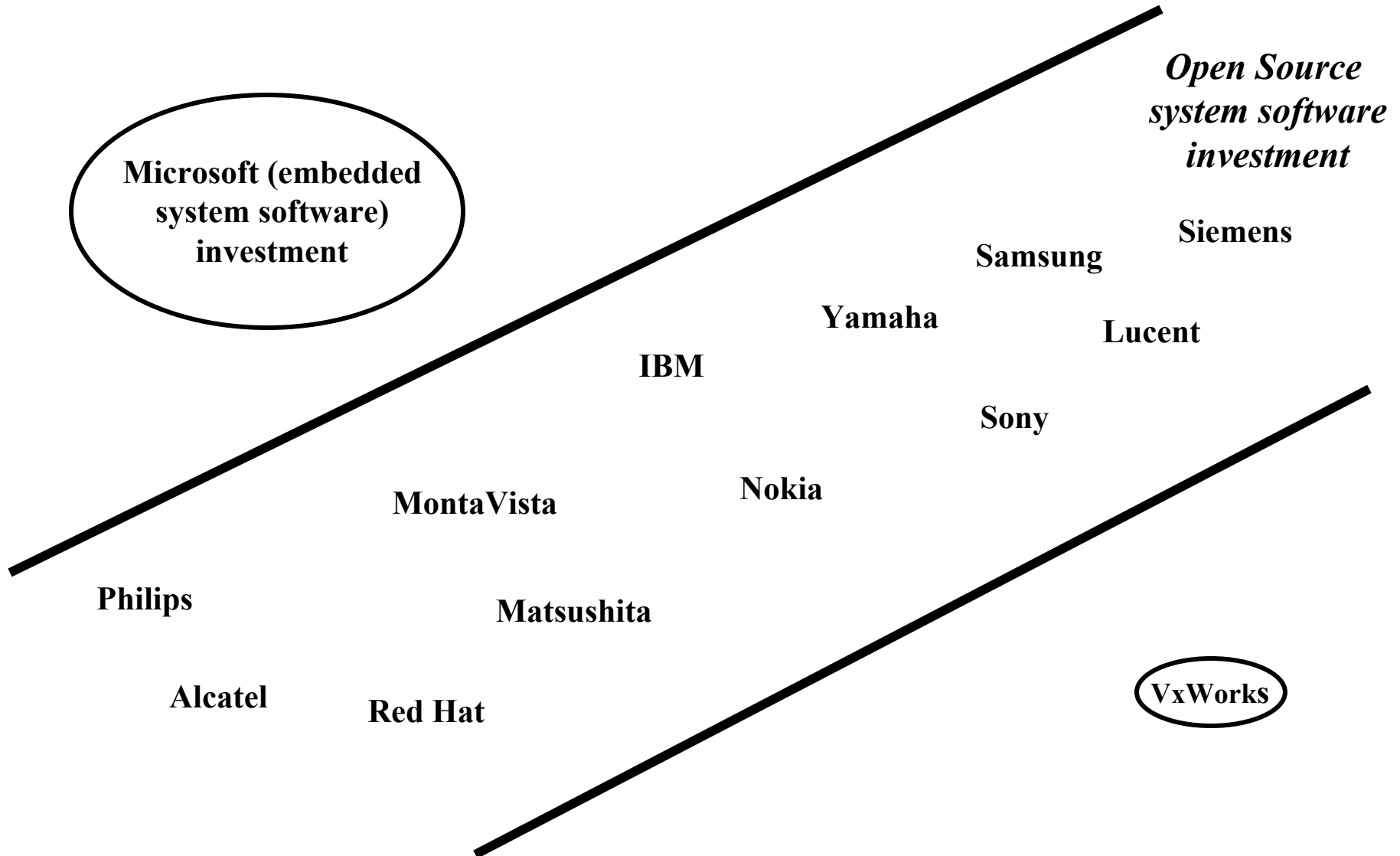
The war has three fronts: servers, embedded, and desktops.

Microsoft investment in embedded system software is at new highs; they will not cede this market to Linux casually!

## *Proprietary system software is doomed*

- ◆ The economic advantages of open source (to all players in the business ecology) are overwhelming.
- ◆ The battle reduces to open source vs. Microsoft. No other vendor can support the sustain investment levels required to compete.
- ◆ Eventually, Microsoft will lose, because of the unique values of open source.

# Relative Investment Profiles



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## **EDAC Emerging Companies Panel:**

EDA Trends You Can't Ignore

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**Charles Welch**

Managing Director

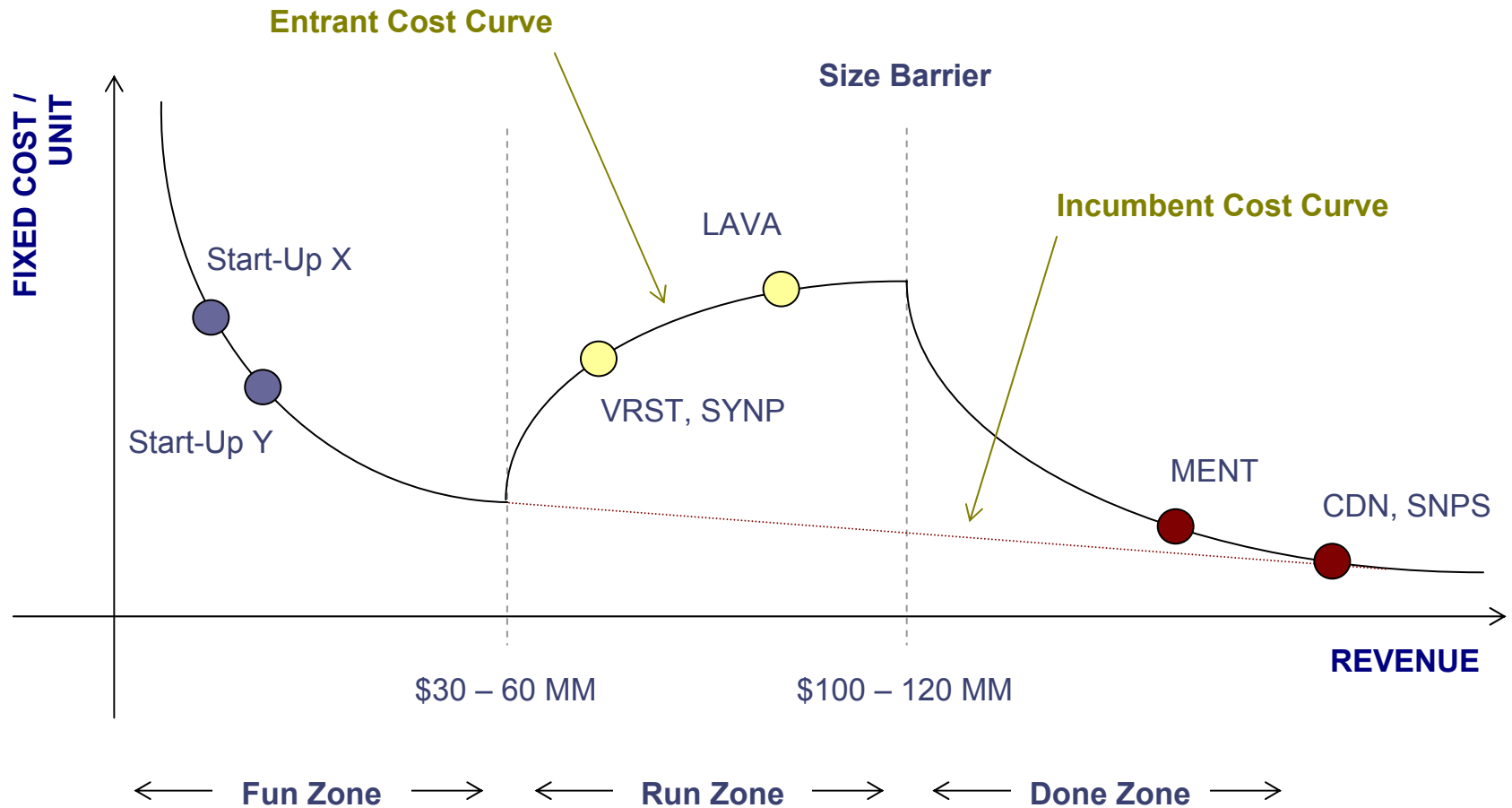


**September 22, 2004**

# Economies of Scale Drive the EDA Industry

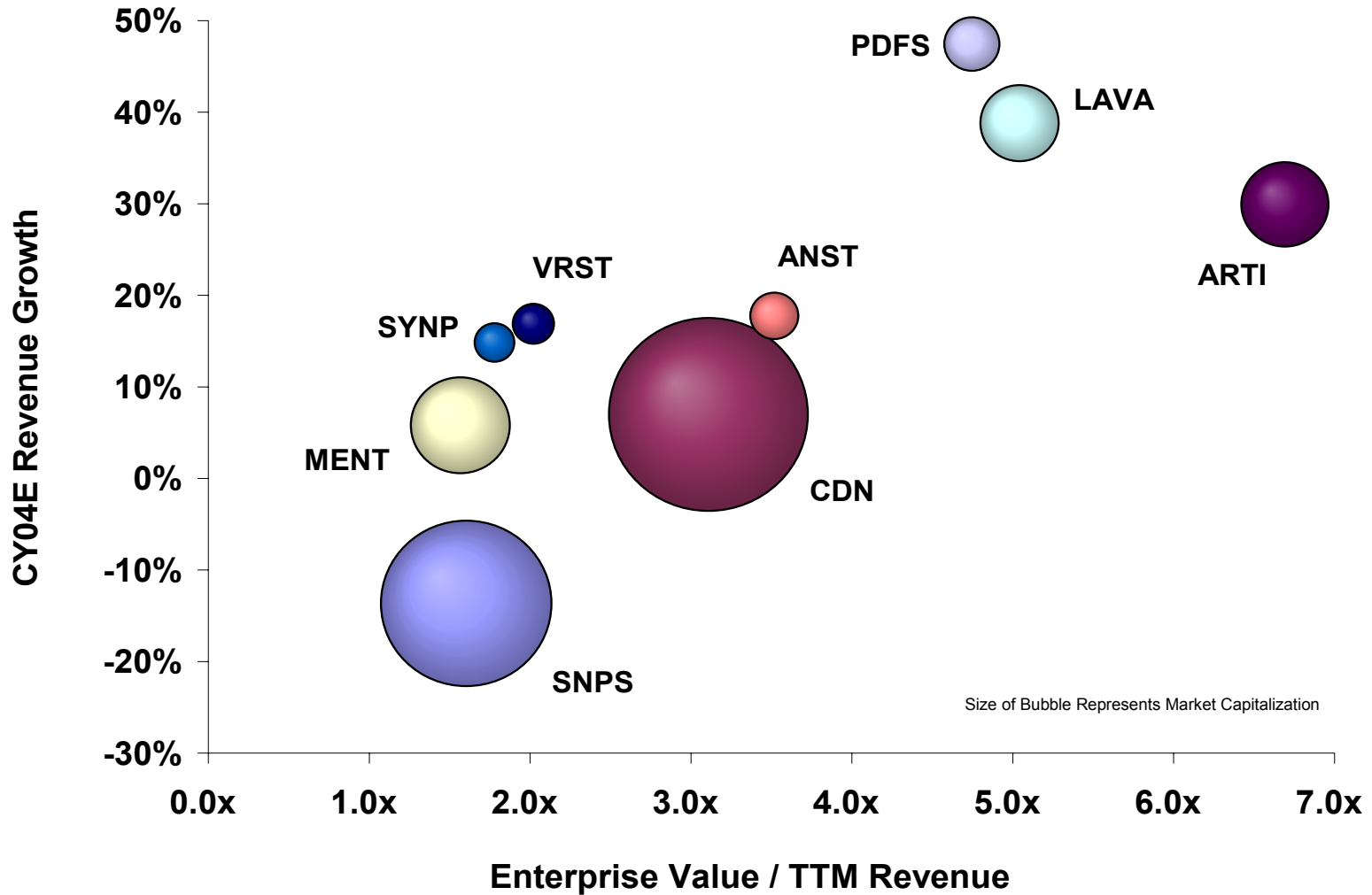
Cost Curves Determine Who Will Survive

Source: Industry data and Credit Suisse First Boston



# Public Markets Reward Growth Over Scale

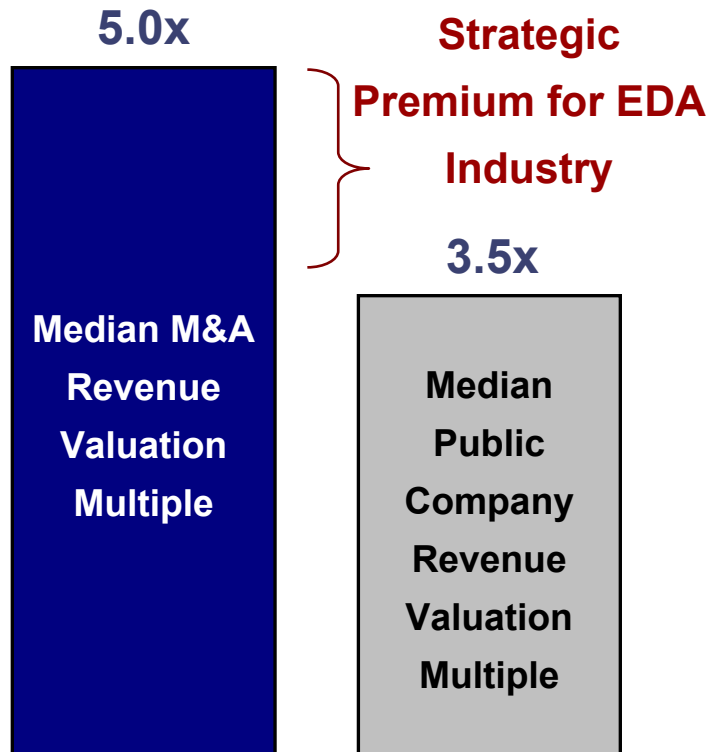
The Larger Vendors Utilize M&A as a Means to Catalyze Growth



# Hence, Acquisition Multiples Tend to Reflect a Strategic Premium to the Public Markets

MEMBER NASD  
MEMBER SIPC

Valuation is a Direct Function of Strategic Fit



## Value Drivers

- Disruptive / next-generation technology complementary to existing design flows
- Demonstrated revenue traction and referenceable customers pushing incumbent vendor to cut a deal
- Partnerships and equity investments already in place with potential buyers
- Competitive process (usually facilitated by an advisor)

Selected Public Companies include: SNPS, CDN, MENT, LAVA, ARTI, ANST, SYNP, PDFS, VRST, NSDA

Selected M&A Transactions include: 0-In, Hier, Neoliner, Mojave, SYCON, Axis Systems, Silicon Metrics, Verplex, Innologic, IDS, WaferYield, K2, Get2Chip, Celestry

## Leading Advisor to the Technology Industry

Source: MergerStat and SVB Alliant

<u>Technology Transactions Under \$250 MM Announced Since 2003</u>	
<b>SVB Alliant</b>	<b>61</b>
Jefferies Group	51
Credit Suisse First Boston	47
Morgan Stanley	43
Houlihan Lokey Howard & Zukin	34
JP Morgan Chase	34
Citigroup Global Markets	33
UBS	29
Bear Stearns	24
Lehman Brothers	24

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<u>All Semiconductor Transactions Announced Since 2001</u>	
<b>SVB Alliant</b>	<b>27</b>
Morgan Stanley	21
Credit Suisse First Boston	20
Houlihan Lokey Howard & Zukin	12
CIBC World Markets	10
Jefferies Group	10
Piper Jaffray	10
JP Morgan Chase	9
Thomas Weisel Partners	9
Goldman Sachs	7