

PHILIPS

Panel Discussion:
How Short Product Life Cycles are
Stirring the EDA Industry?
“Trends You Can’t Ignore”

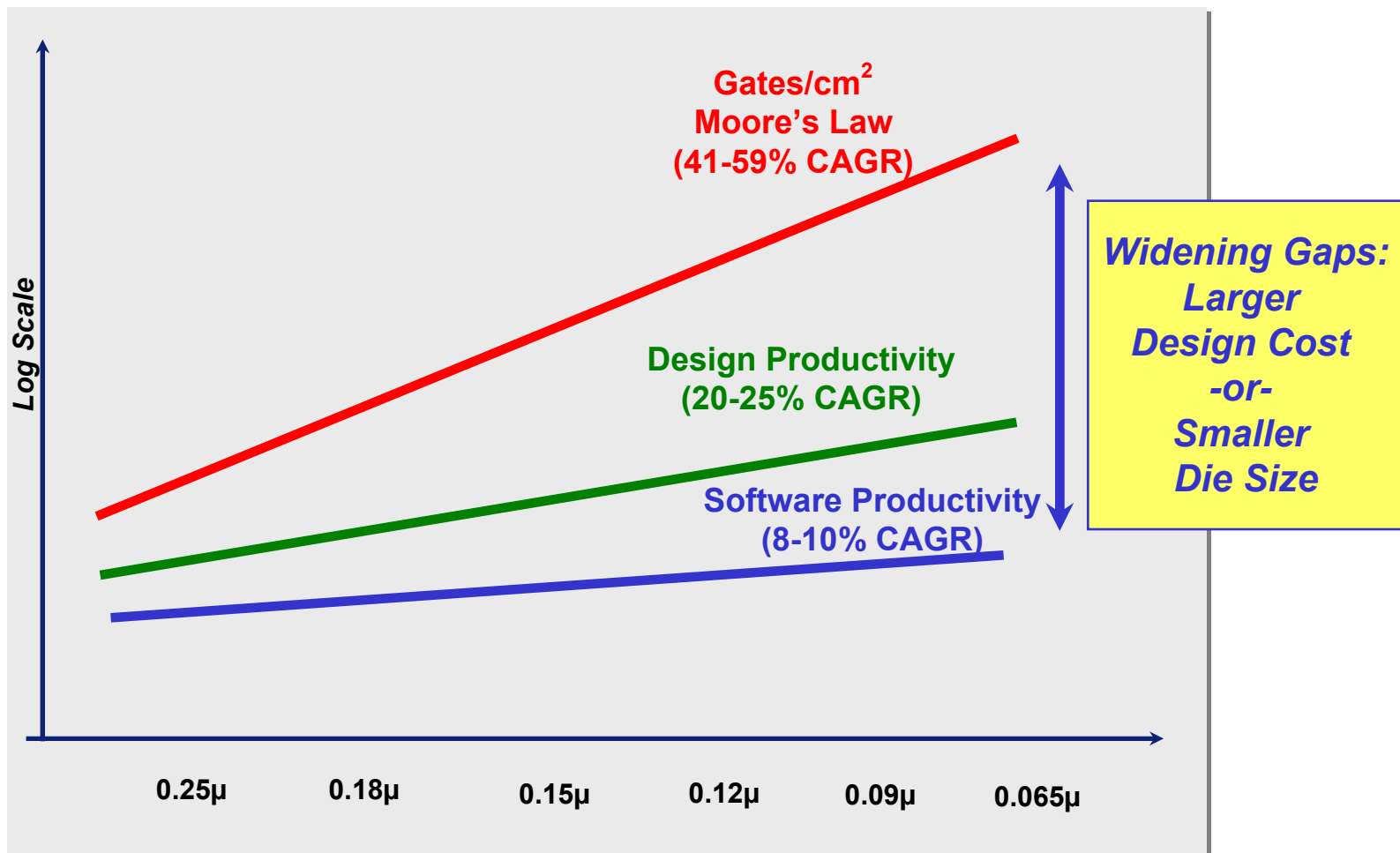
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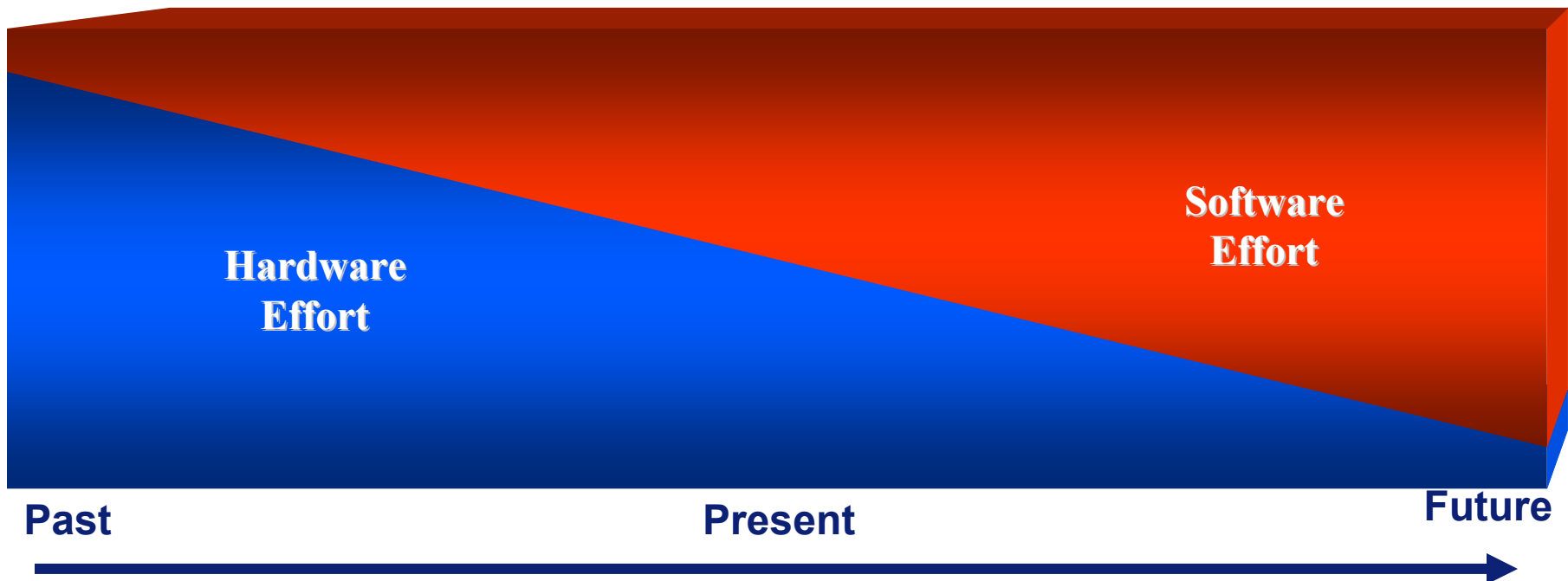
Sept. 22nd, 2004

Design Productivity Gap



Why the Software Productivity Concern??

- In the end; if we solve the HW design productivity and fail to address the SW productivity we have accomplished little.
- **System design productivity** is the objective.



The Trends:

- Productivity shortfall manifesting itself as an increasing average design cost from generation to generation – Probably doubling every four years (\$10M and Growing)
- Targeted production revenue needs to be 10X the development since system R&D spending is generally held to 10% of revenue
- Fewer sockets can produce the targeted revenue and therefore we see fewer design starts
- More SW programmability/re-configurability is required to cast a bigger production revenue shadow and address time to market

SOC Key Issues

Correct Functionality

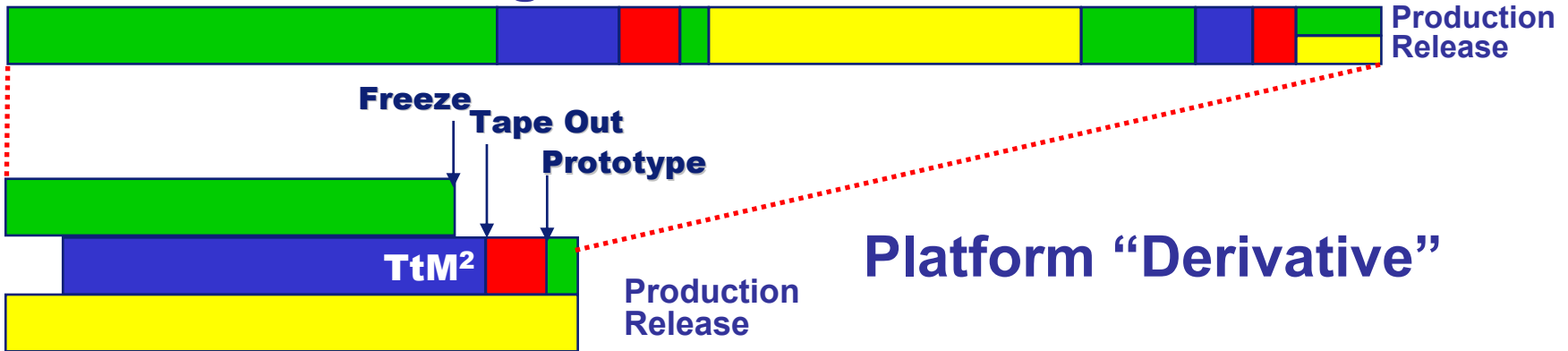
Cycle Rate	Debug (Hrs)	Debug Time	Technology		
1	1	1 Hour	Silicon Reference Design	Simulation	Hardware
10^{-1}	10	~1 Working Day	FPGA		
10^{-2}	100	4 Days	HW Emulator		
10^{-3}	1,000	1.4 Months	Throughput Model	Simulation	Software
10^{-4}	10,000	1.2 Years	Transaction Model		
10^{-5}	100,000	~12 Years	Cycle Accurate Sim Model		
10^{-6}	1,000,000	>1 Lifetime	RTL Model		
10^{-7}	10,000,000	~1 Millenium	Gate Level Model		

Hours of Testing Experience are Required

A Reference Design is the Least Abstract & Most Accelerated

Platform “Derivative” Design

Conventional Design Process



- **Hardware Software Co-Design**
- **Physical Co-Design**
 - Change Friendly Design Process
 - Timing Closure Friendly Architecture
 - Handoff Friendly Methodology

Evolution of SoC Enemy #1

- When I started to design ICs **PERFORMANCE** was my biggest concern.
- As I matured into management **COST/DENSITY** was my biggest concern.
- Now **POWER** has emerged as my biggest concern.
 - Why?
 - Interesting Observations About Designing For Low Power!

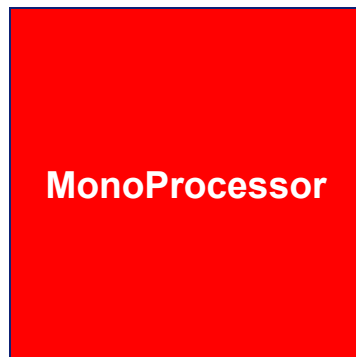
Some Shocking Observations!

- **How much Power would a Performance Focused IC Consume?**
 - **3GHz Pentium 4 runs $>75W = 50A * 1.5V$**
 - **Only about 10% of the chip runs at 3GHz**
 - **If the entire chip were run at the Compute Engine speed the chip would consume $> 500W/square\ cm$**
 - **Extrapolation of this trend indicates future technology will exceed $1KW/square\ cm$.**
 - **I am told that this is same power density as nuclear reactor**
- **Practical Limits:**
 - **Consumer Electronics $\Rightarrow 2.0W$ to $4.0W$**
 - **Mobile Electronics $\Rightarrow 0.2W$ to $0.4W$**

Which Wish Should Be Granted?

Wish #1

World's Fastest
"Do All"
MonoProcessor



Wish #2

Simple Control
Processor and "Farm"
of Streaming Engines



Orchestra Analogy

RISC Processor = Conductor

Streaming Processors = Musicians

Information Pipes = Patrons



- **Best Computation Per Square Millimeter**
- **Best MediaStones Per Mille-watt**
- **Turning into industry trend**

