

Cadence Design Systems

Ray Bingham, President & CEO
February 2003

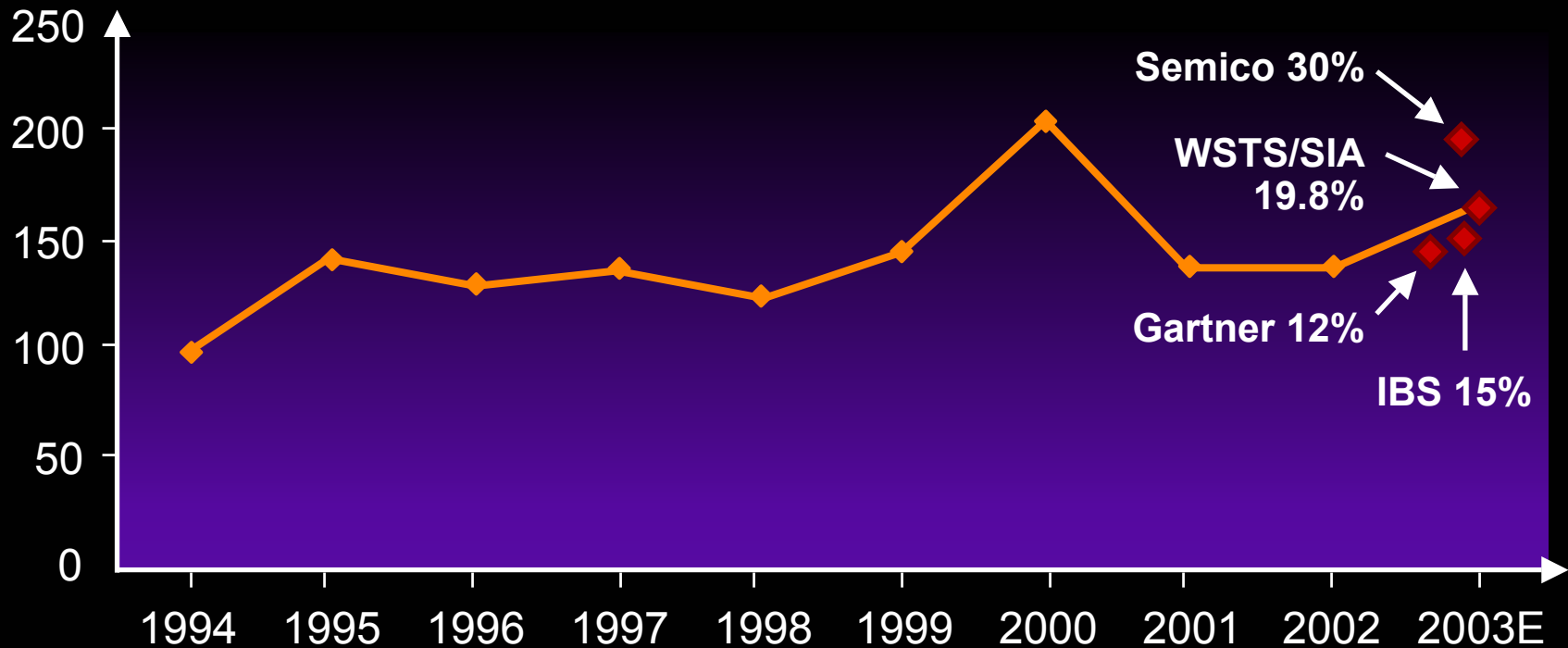
Safe Harbor Statement

The following discussion contains forward-looking statements, and our actual results may differ materially from those discussed here.

Additional information concerning factors that could cause such a difference can be found in our 2001 10-K for the period ended December 29, 2001, and our 10-Q for the period ended September 28, 2002.

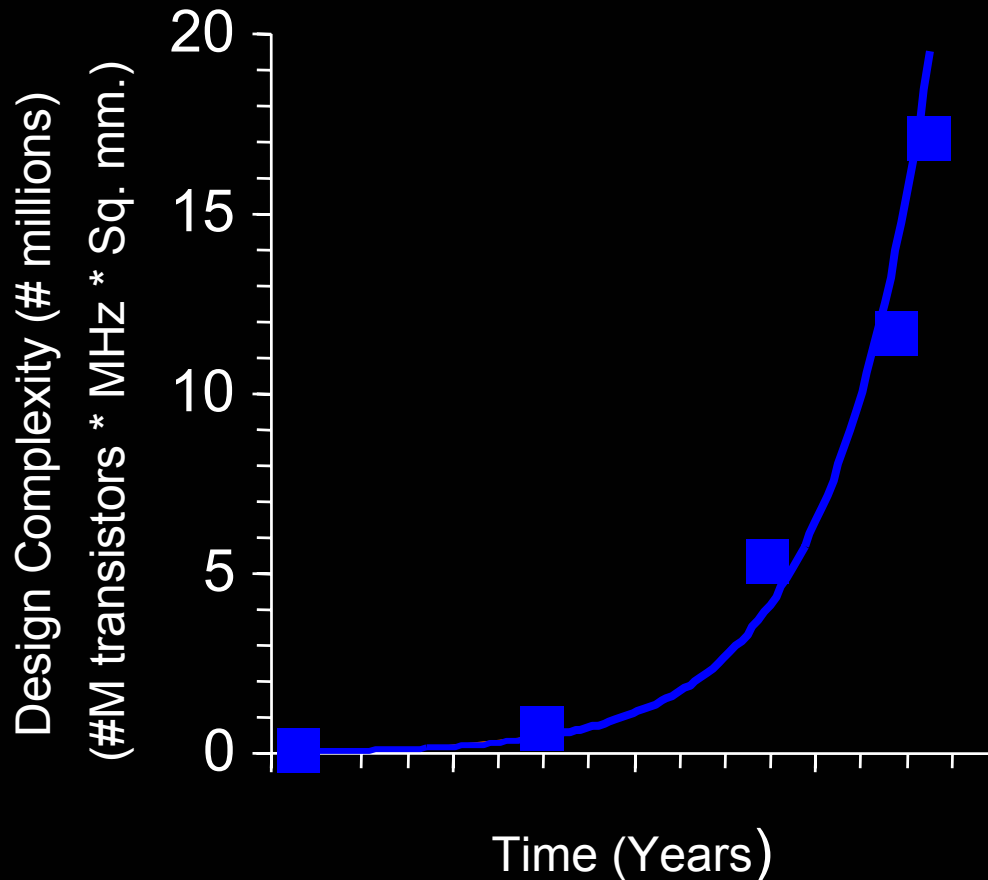
Light at the End of the Tunnel: Semiconductor Recovery Projected

Semiconductor Revenue



Source: WSTS/SIA; Gartner; Semico

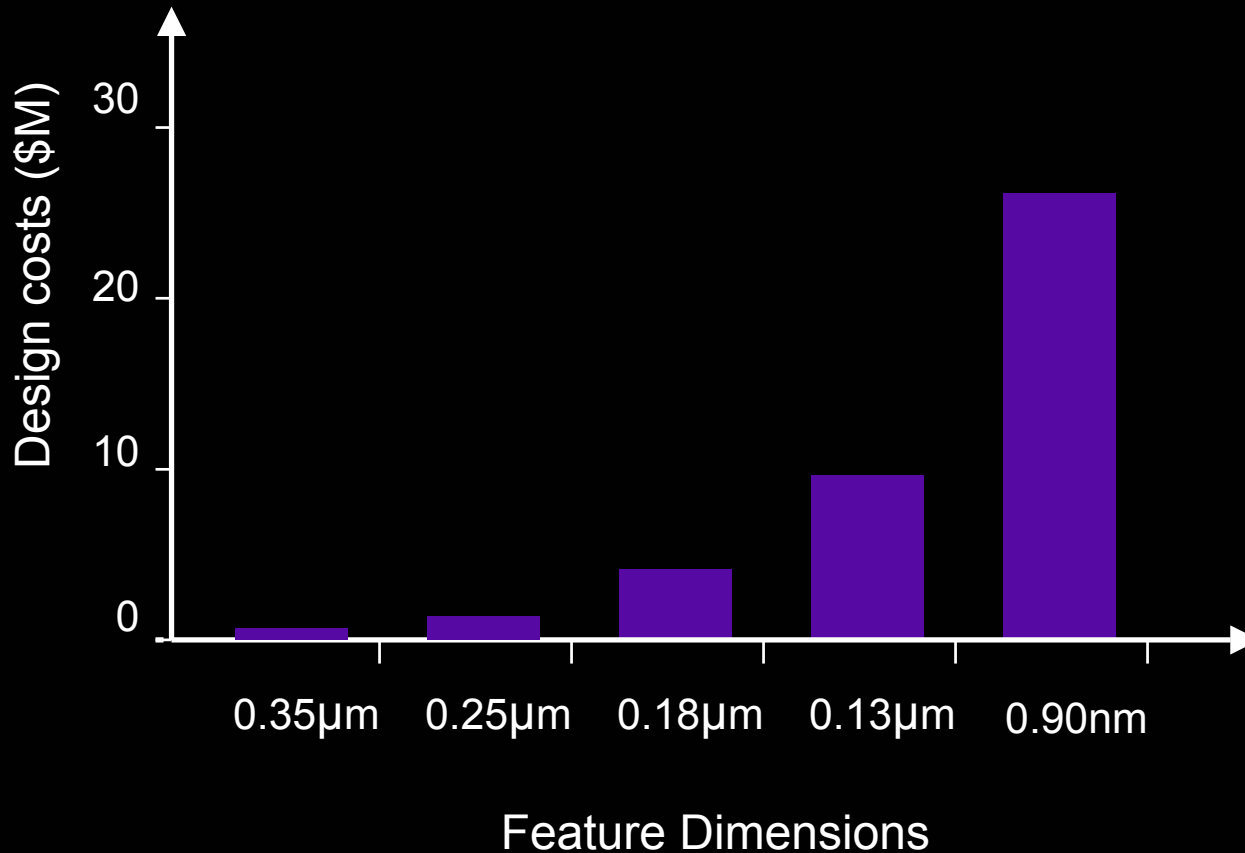
Design Complexity Increasing



- 30M – 300M transistors
- 10 – 30M wires
- 10 x 10 – 18 x 18 sq. mm
- 200 – 900 MHz clocks
- 2,000 I/Os
- 200 MHz – 3.125 Gb/s I/Os
- 5 – 25 watts
- 2 – 15 amps

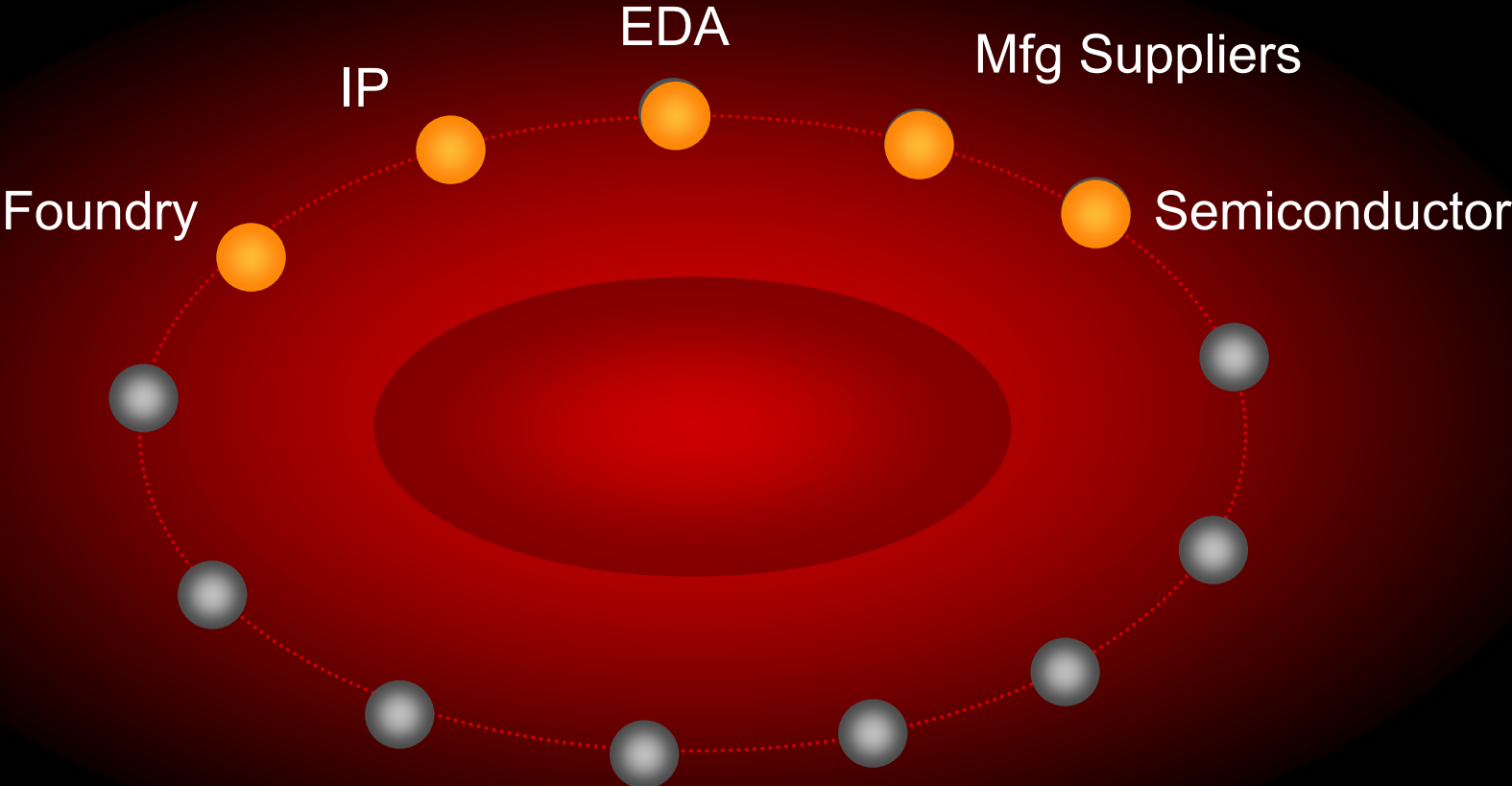
Source: Cadence Design Foundry

Semiconductor Design Costs are Rising Exponentially



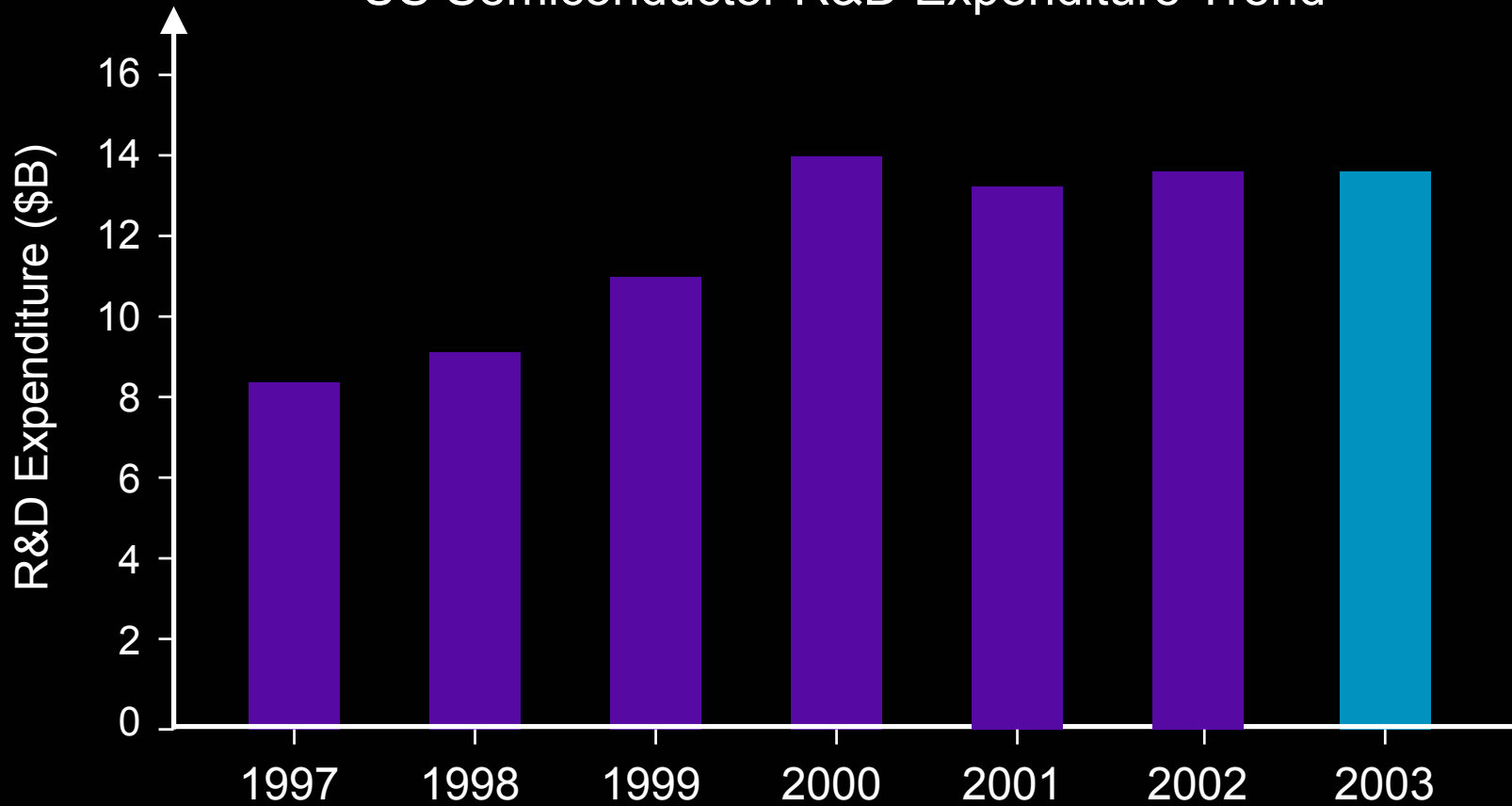
Source: Gartner

Integrate the Design Chain



R&D Sustained Through Downturn

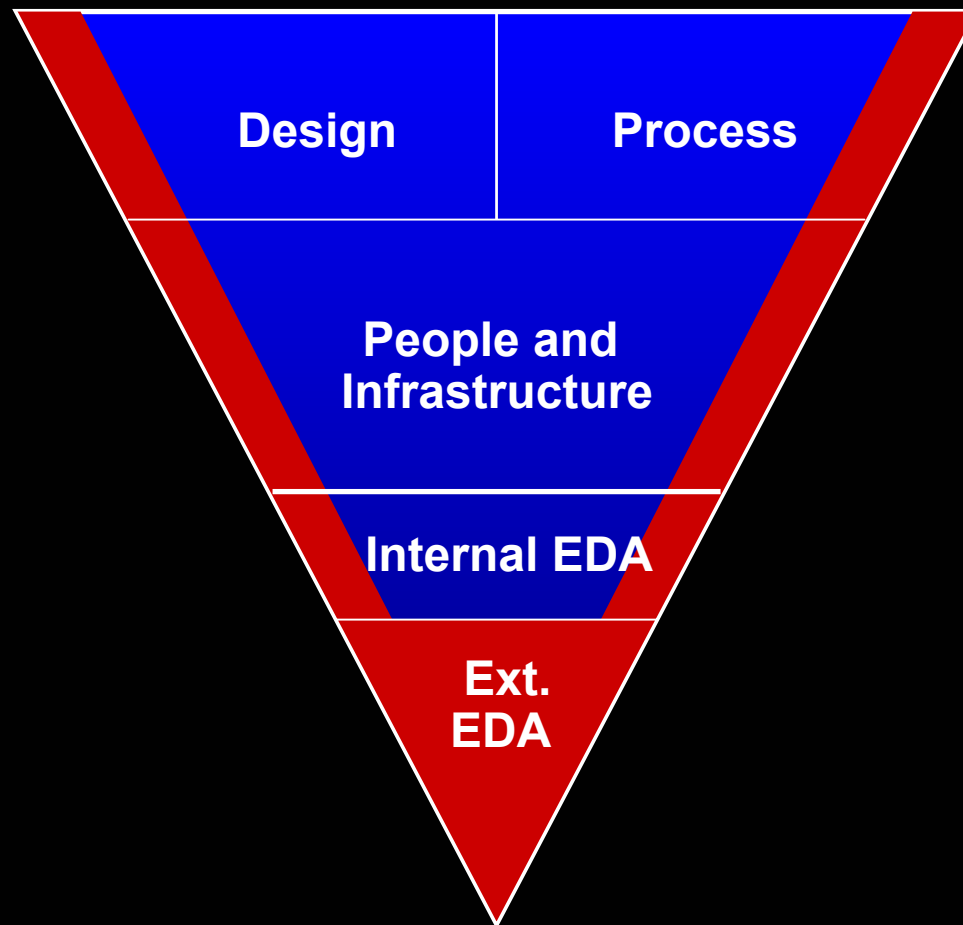
US Semiconductor R&D Expenditure Trend



Source: ICInsights

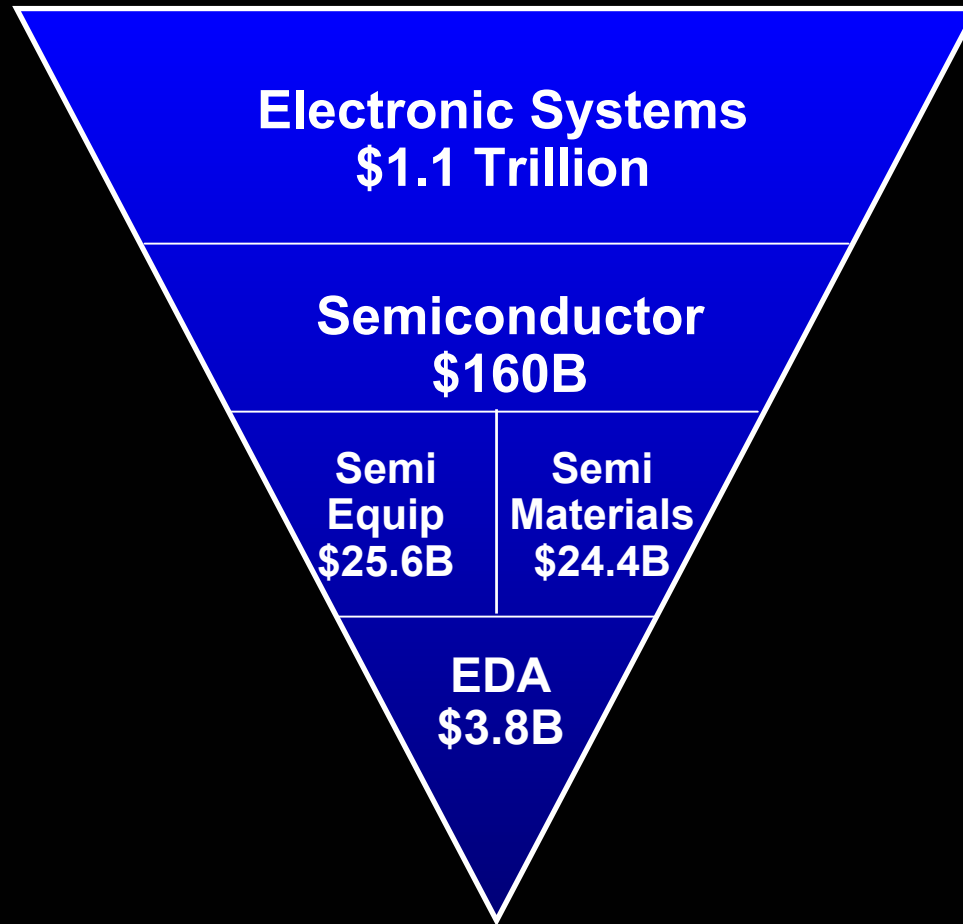
Reducing Customers' Total Design Costs Grows EDA Opportunity

Electronics R&D



Source: ICInsights; Gartner;
EDAC forecast estimates

Electronics Hinges on EDA



Source: ICInsights; Gartner;
EDAC forecast estimates

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