

The Metrics of Success

Design Leadership is a key profitability metric for IC companies

In 2002, International Business Strategies (IBS) researched the relationship between the profitability of semiconductor companies and their design capabilities. The study showed a direct correlation between the design capabilities of those companies and various key financial metrics—profitability, stock price, and revenue ranking. The IBS research proved that the financial results of semiconductor companies are clearly linked to their design capabilities.

In 2004, IBS updated the earlier study to gauge the effects of changes in the economy and the technology that have taken place in the interim. Not surprisingly, the 2004 study found that increases in design cost, a reduction in the number of design starts, and the adoption of finer geometries and larger wafer sizes have affected the financial performance of semiconductor companies around the world.

Similarly in that same period between 2002 and 2004, the IBS study found that EDA spending declined as a percentage of most R&D budgets, which in turn has led to the present, well-established need for better design productivity. The study also reports that those IC vendors able to maintain leadership-level design capabilities even in the downturn continued to show strong financial performance within their targeted business areas and market segments. As in the 2002 study, the 2004 report indicates that analyzing the design capability of an IC company can help determine the profitability and market position for the companies, and a company's design capabilities are directly related to its market valuations.

RETHINKING BUDGET LIMITATIONS

In light of these findings, many feel that the single most important challenge facing the IC industry today is to enhance design capabilities by making more effective use of third-party EDA tools. First, however, the industry needs to move beyond existing tool budget limitations, which are based on previous tool expenditures. The IC industry needs to begin to quantize the benefits of third-party tools to deliver the necessary proof to their internal CAD organizations for increased flexibility in EDA tools budgets.

The EDA industry is facing challenges as well. It needs to stop watching revenues increase and decrease in response to fluctuations in the health of its customers, and work instead towards increasing third-party tool expenditures as a percentage

of IC and electronic company revenues. We've reached a critical juncture where the EDA industry must learn to convey the benefits of its offerings to a broad range of customers using the now-established link between the use of third-party tools and improved financial metrics for semiconductor companies.

Time to market is a critical competitive metric for most market segments. Similarly, a key issue for IC companies is how to produce a product within a required market window. The IBS study showed that competitive differences in the time-to-market capabilities of IC vendors are directly related to how effectively they use their EDA tools, as well as the level of training and skill of the design team.

FACTORS IN COMPLEXITY

A growing number of IC companies now rely on pure-play foundries for their manufacturing, as the costs of establishing internal wafer fab capabilities have become prohibitively high. With this move away from in-house manufacturing, in-house design capabilities become the single, overriding competitive differentiator for IC companies.

Additionally, design problems at 0.13 micron are lengthening the time required to bring new products to market, especially for chips containing mixed-signal functionality such as high-speed I/Os. IC functionality is, however, just one among several major building blocks in the overall system. System-level design concepts must also be addressed as customers increasingly migrate to platform-based design solutions. As IC vendors move into system architecture and chip-set solutions, the design tools must support this trend.

Today the IC market is in a growth phase, with capacity shortages predicted to become severe in late 2004 and 2005. These capacity shortages will result in price premiums for ICs and increased profits for IC companies. The IBS study notes that capacity shortages will place an increased emphasis on yield optimization and chip area minimization in order to increase output from wafer fabs. For example, a wafer fab that produces \$1 billion in IC products will generate \$100 million in increased revenues if the chip area in those products is reduced by just 10 percent.

Case studies examined to support conclusions in the IBS study were done for designs at 0.13 micron with a high amount of

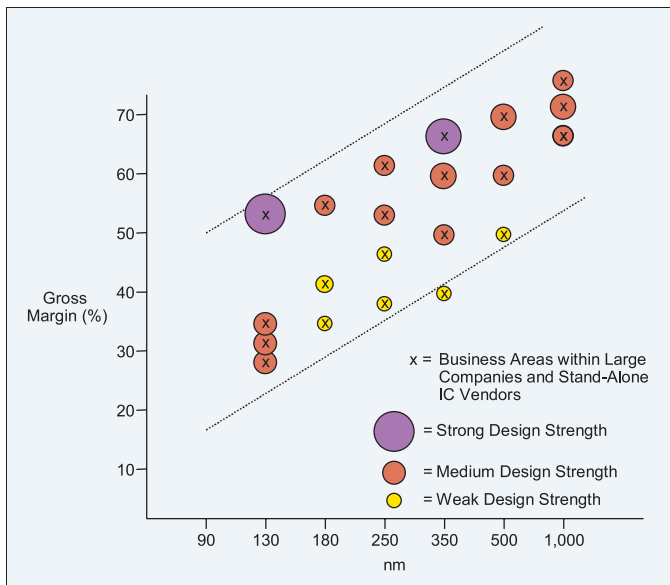


Figure 1—Gross margins and design strength per feature dimension.

logic. The gate count levels of the designs ranged from 5.8 million to 12.4 million. Beyond size considerations, other challenging factors in the designs included next-generation performance requirements and the integration of demanding functions such as high-speed interfaces, low power, area minimization, and so forth. The results in the study produced difficulty factors in the range of 2.33 to 8.70, indicating a significant variation in the ability of IC vendors to bring new designs to market within short time windows. (see Figure 1)

The case studies also indicates that there is a direct correlation between complexity and cost, as well as between complexity and time to completion. The ratio of complexity to time to market for new designs was chosen as an indicator of the competitiveness of IC vendors. The IC vendors that have the best design capabilities are able, according to the IBS study, to bring their new products to market at the lowest cost and in the shortest time, thereby obtaining price premiums for their products.

The ramp-up of 0.13-micron and 90-nanometer designs has been slow due to design difficulties inherent at these nodes, but technology indicators suggest that problems at 0.13 micron are finally starting to be addressed. IBS has found that the companies that are placing a strong emphasis on procuring the latest design tools, training their design engineers, and establishing close links between their design and process databases are the ones who are achieving the first successes at 0.13 micron.

At the same time, IBS observes that IC product costs are linked primarily to chip area, while major trade-offs must be made at design closure between timing, power, and functionality. These trade-offs involve increased risk for the design team as the

complexity of the design increases. Within this context, effective design tools, again, serve as a major asset in obtaining closure, and extensive training in the use of these tools can significantly help to reduce the risk.

Meanwhile, the situation is further exacerbated as companies begin to invest in design centers in emerging countries. The growing shortage of highly qualified IC design engineers which results from this migration generates additional pressure in meeting market windows. Again, advanced third-party tools can help to alleviate these pressures.

THE CASE FOR EDA

The IC industry is in a recovery mode and, as mentioned, is expected to grow in 2004 and 2005. Accordingly, the EDA industry should find itself in a growth position over the short term. However, maintaining and nurturing longer-term growth will depend on EDA's ability to fundamentally change its relationship with its customers, the IC vendors. As R&D expenditures increase, there will be a corresponding increase in EDA expenditures if, and only if, the customers are successfully made to understand how the tools increase the value of their own in-house design capabilities.

Today, EDA tool licenses represent only 1 percent of revenues for many IC vendors. However, a significant upside potential exists for the EDA industry if the value of the design tools can be demonstrated effectively to the customers. Although EDA sales strategies have traditionally focused on technology metrics, it's singularly important now to add the potential improvements in financial metrics to those sales arguments if EDA intends to reap the benefits of increased revenue streams.

The IBS report states that an EDA budget ought to be based on the actual benefits it will accrue for the IC vendor in terms of increased productivity of its design engineers, higher IC revenues and profits, and higher market valuations. For this to be fully understood and carried out, the decision process must be elevated to the top-level management within an IC company.

Additionally, according to the study, revenue per design will need to increase in order to cover the increased costs of a design. IBS predicts that the total number of IC designs starts worldwide in 2004 worldwide flat or down, but that design costs will rise as complexity grows.

Therefore, shareholder value for a semiconductor company will be directly related to the short-term emphasis placed on design capabilities. The emphasis IC vendors choose to place in the long run on establishing design leadership will, in fact, provide major

payback to shareholders. Thus, design leadership will become a key metric for projecting the future competitive positions of IC companies, and a matter of great interest to potential investors. While it's certainly important to have access to appropriate wafer fab capabilities, IC vendors will increasingly need to achieve leadership design capabilities to be financially successful.

POTENTIAL FOR GROWTH

The EDA industry has high growth potential if the financial benefits of leadership design implementation capabilities are better understood by the IC and electronics industries. IC design costs now account for 10 to 15 percent of IC revenue, and are predicted to increase to 20 percent of revenue in the future. Typically, EDA tools account for 10 percent of design costs, or 1 to 1.5 percent of IC revenue. As IC revenue accounts for 10 to 20 percent of electronic system manufacturers' revenue, it's clear that EDA tools currently account for only 0.1 to 0.2 percent of equipment revenue.

Current spending levels on EDA tools are not what they should be. The IBS study bears this out in clearly demonstrating that gross margins, market valuations, and competitive positions for IC vendors are tied to in-house design capabilities and the effective use of EDA tools. It is incumbent upon the EDA

industry to communicate these results, since they directly affect the performance of our companies and the progress of both the EDA and IC industries.

Design efficiency and yield improvements are essential for a company to maintain a competitive stance in a crowded market. EDA tools provide the logical route to accomplish these ends.

The ability of EDA technology to help wafer fabs ramp up faster has a far greater financial impact on IC vendors than the cost of design tools. EDA tool costs are generally 10% of the cost of a design project. Shortening the time to ramp up a new 90nm fab can represent hundreds of millions of dollars for an IC vendor.

Note: The entire report from International Business Strategies, Inc., "The Continuing Importance of Design Capabilities to IC Companies", was made possible through the support of the EDA Consortium and edacentrum e.V. The report is available for free download at <http://www.edac.org>. ♦

Jacques Benkoski is president and CEO at Monterey Design Systems. He is also vice chairman of the EDA Consortium.

Chip Design — the only print & online publication 100% focused on the advanced IC design market

Subscribe FREE at www.chipdesignmag.com to access the latest tools, technologies & methodologies.

Editorial coverage includes:

Tools and Languages

- Design (ESL, RTL, Gate, Netlist, Analog/Mixed-signal, RF)
- Implementation
- Design for Manufacturing
- Verification
- FPGA tools
- Design & Verification Languages
- Test

IP and Libraries

Methodologies

- Methodologies
- Standards
- Verification

Semiconductor Platforms

- Programmable Logic
- ASIC/SoC
- IP
- Libraries
- Structured ASICS
- Foundries



Affiliate Sponsors



Visit www.chipdesignmag.com today to download current and back issues of Chip Design—FREE!