



HW/SW Co-verification in Teradyne

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What is Teradyne Semi Test?

- **World leader in high-efficiency low-cost test**
 - **Logic, RF, analog, power, mixed-signal, memory, SoC**
- **Primary supplier for world's leading electronics companies**
- **A tester combines multiple densely loaded boards and a large SW package**

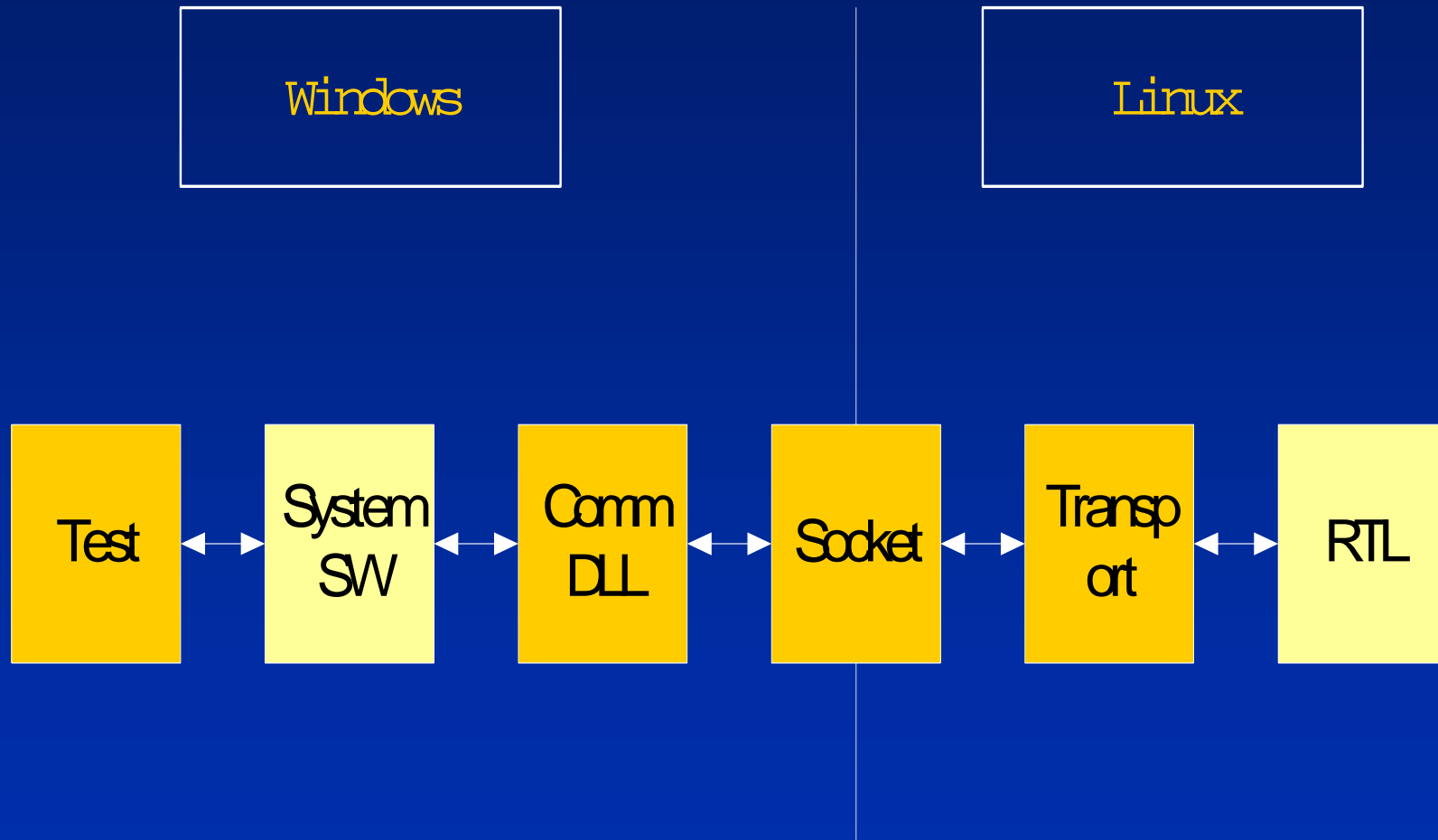
Why Does Quality Matter?

- **Testers are always on critical path**
 - **Work 24/7**
 - **Any problem damages customer's program severely**
- **Clock starts ticking as soon as the tester is installed**
- **Customers always have a choice**

How Do We Assure Quality?

- **Verification!**
 - Multi-level HW verification
 - Off-line SW verification
- **Co-verification!**
 - Co-simulation
 - Early platform for SW development
 - Mutual adjustment of SW and HW specs
 - Lab entry with debugged SW
 - Debug environment for system-level problems

How Do We Do Co-Verification?



Why Don't We Use Modeling?

- **Co-verification is much more than just an early platform for SW development**
- **No need in architectural modeling**
- **Model development is quite an effort**
- **Existing SystemC IP libraries don't help**

How Can EDA Vendors Help?

- **User-friendly socket utilities or some other support for 2-OS environment**
- **Emulation?**
- **Faster simulators, cheaper licenses, better support!**

The End

Thank You For Your Attention