Manufacturing Technology Trends and Implications for Design

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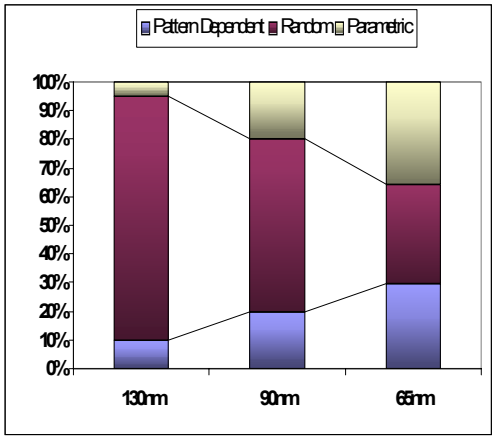
Process Benchmark

- **130nm SOC world class yields at maturity level**
- **90nm SOC world class yields becoming mature**
- **65nm SOC world class yields capable of early manufacturing**
- **Implications:**
  - 90nm is economically attractive relative to 130nm for many logic applications
  - 65nm volume production will be here within 1 year+

65nm and Below Yield Challenges

High Yield and Performance Variability

- **Very small litho process window**
  - High risk of product to product variability
  - Equipment differences and PM cycles will have more dominant effect
- **Stress engineering create more performance variability**
  - Layout dependant stress mechanisms
  - Film control is critical
  - Modeling is more difficult
- **NiSi abnormalities will create transistor variability**



Yield Loss Breakdown

Design rules, layout design styles, and physical synthesis methods will need to embed layout consistency

Trends in Manufacturing and Implication for Design

New Optimization Variable: Good Die per Wafer

- **The old paradigm - smaller is better**
- **The new paradigm - maximize of good die per wafer**
- **Examples of the new paradigm**
  - Logic redundancy
  - Restricted orientations and pitches
  - Regular arrays
- **Implications**
  - DFM is more than doubling vias and contacts
  - Need to simulate yields across all levels of the design flow
  - Need accurate characterization of process capability over time