

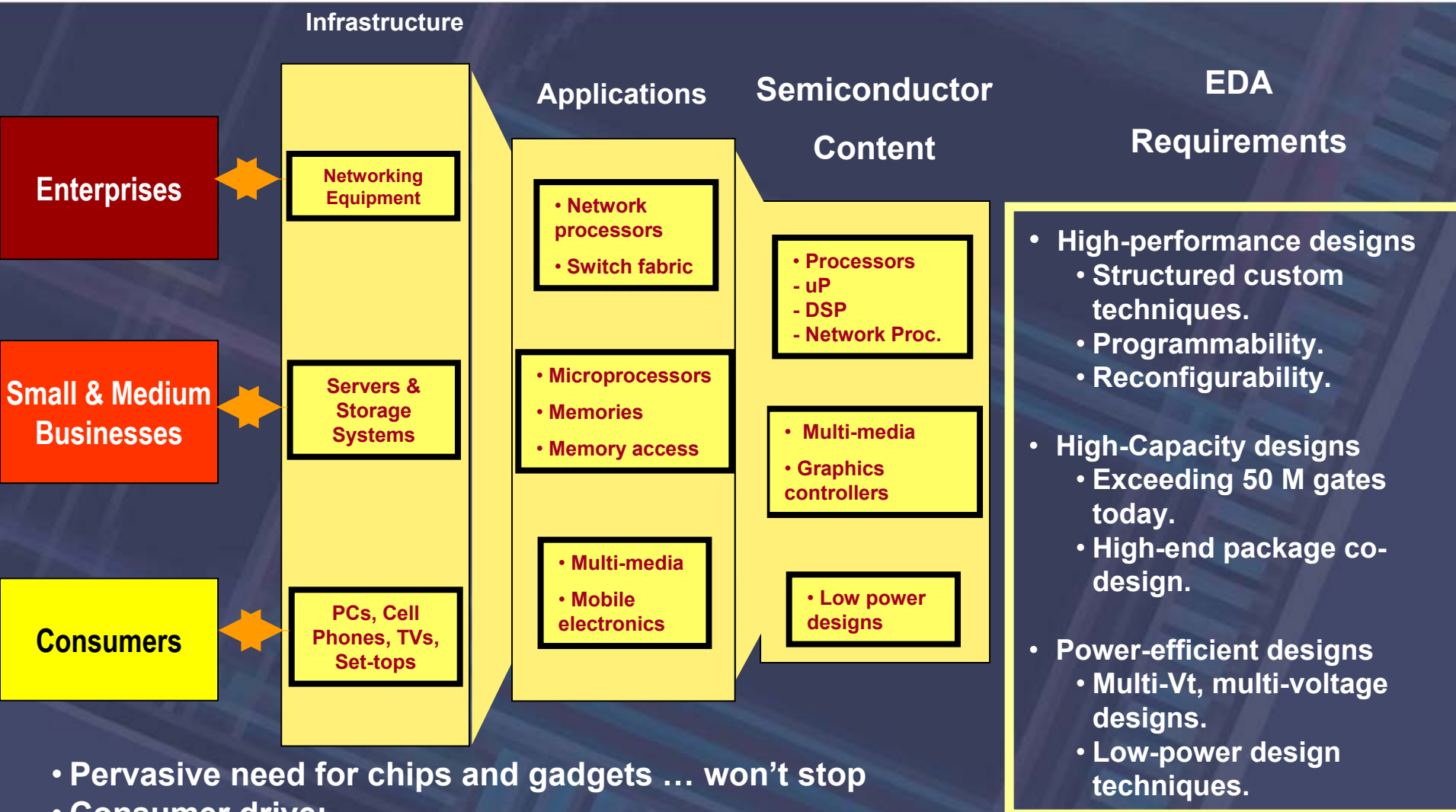


The Fastest Path from RTL to Silicon

The following discussion contains forward-looking statements, and our actual results may differ materially from those discussed here.

Additional information concerning factors that could cause such a difference can be found in Magma's Annual Report on Form 10-K for the year ended March 31, 2003, in Magma's Quarterly Report on Form 10-Q for the quarter ended December 31, 2003, and in subsequently filed reports. Forward-looking statements speak only as of the earlier of the date first published or the date hereof. Magma disclaims any obligation to update forward-looking statements.

Good News: Semiconductor Food Chain



- Pervasive need for chips and gadgets ... won't stop
- Consumer drive:
 - Earlier adoption of DSM technology.
 - Wireless Web revolution.

Bad News: Shrinking Profitability from Silicon Design

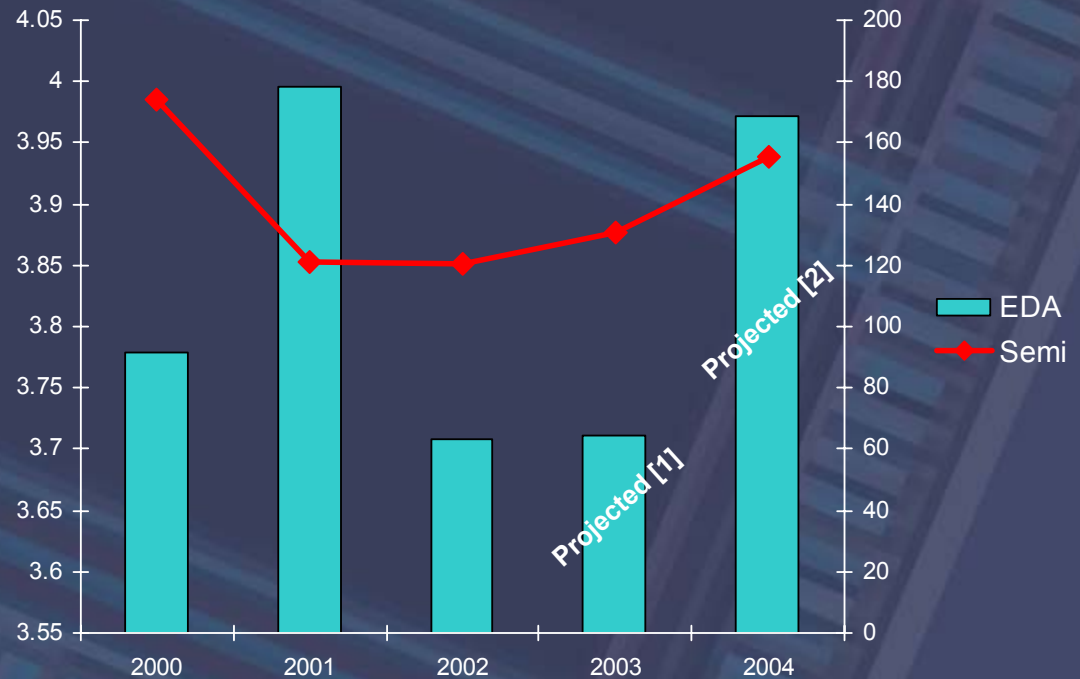
- **40 M gate designs**
 - 18mm X 18mm, 2000 I/Os, 500Mhz
 - Approximately 4M lines of RTL
- **50+ engineers**
 - Experts in synthesis, P&R, signal integrity, power analysis, design closure
 - Analog, digital verification
 - Closing loop with eqpt, manufacturing
- **\$80MM investment**
 - EDA is looking like financial software – no instantaneous ROI
 - Requires \$160MM in 2 years to realize break even
 - Where is the killer application for this??

EDA Needs to Make Moore's law economically infeasible

Forecasts: EDA and Semiconductor Revenue

- **Quick forecast:**

- EDA revenue from EDAC data.
- Semiconductor revenue from Gartner & IBS.



Notes:

[1] Presumes 4Q 2003 same as 4Q 2002.

[2] Presumes 7 percent growth over 2003.