ANALYSIS OF THE RELATIONSHIP BETWEEN EDA EXPENDITURES AND COMPETITIVE POSITIONING OF IC VENDORS FOR 2003

A CUSTOM STUDY FOR EDA CONSORTIUM AND edacentrum e.V.

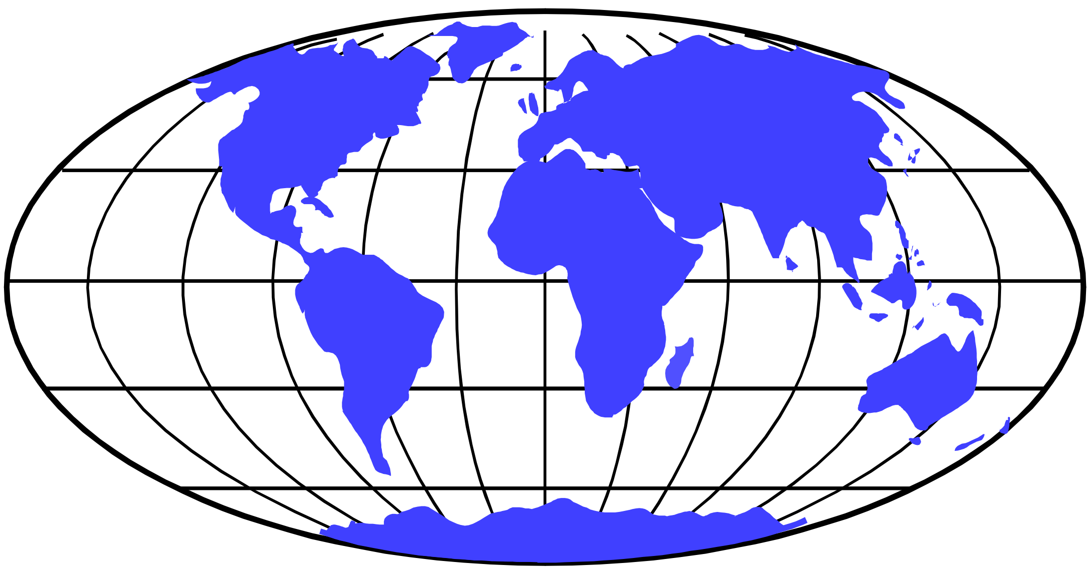

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TABLE OF CONTENTS

Page

1.	Executive Summary	1
2.	Introduction	5
3.	IC Market Issues and Trends	10
4.	Impact of Design to IC Vendor Financial Performance	22
5.	Design Cost Strategic Issues	37
6.	Conclusion	53

The following are the issues between EDA expenditures and the competitive positioning of IC vendors:

- The IC market is in a growth phase, and capacity shortages are becoming more severe. The IC market is recovering, with the trend toward increasing R&D expenditures.

- Although EDA tool spending has not shown the same increase as R&D expenditures, there is the expectation that EDA spending will also grow.

  The EDA industry needs to set prices based on value, which can increase market share as well as the total market. However, the value of design tools has not been established, and the EDA industry needs to change this so that the IC industry understands the value of EDA tools and provides larger budgets.

  The EDA industry has a major financial opportunity to address design problems at 0.13µm and 90nm technologies. Leverage from powerful design implementation capabilities becomes very large at 90nm and even greater at 65nm.

- IC vendors with strong financial performance have ensured leadership design implementation capabilities within targeted business areas and market segments. It is significant that it is not feature dimensions but design implementation capabilities (based on customer inputs) that is linked to the generating of high profits (gross margins) by IC vendors.

Low gross margins and high product development costs of advanced feature IC designs are key indicators that the global IC industry must dramatically increase design engineering productivity.

- Design strengths, ie, EDA tool expenditures, training in use of tools, emphasis by top management on design capabilities, etc, are needed to address current design problems and will be in even greater demand as feature dimensions shrink, ie, 90nm.

- Future requirements of design concepts need to be balanced against the short-term needs of quickly bringing new IC designs to market.

- There continue to be intense pressures to reduce EDA licensing expenditures among all IC vendors.

- Time-to-market for new IC designs is lengthening, even with an increase in the head count of design teams.

  Time-to-market requirements necessitate significant enhancements in design productivity.

- It is critical to determine the factors for growth of the EDA market based on customer needs.

Design capabilities become key factors in revenue leverage of the IC industry because of increasing costs and the strategic importance of product positioning leadership. The analysis of design implementation capabilities of IC vendors provides a basis for determining profitability and market positioning in future, which will directly relate to market valuation.

The business environment issues include:

- The IC market is in a growth phase, with capacity shortages becoming more severe. Capacity shortages will result in price premiums in the IC industry and the ability to increase profits.

  Capacity shortages also place increased emphasis on yield optimization and chip area minimization because of the ability to increase output from wafer fabs. ***If chip area is reduced by 10 percent, a wafer fab that produces $1B in IC products can generate increased revenues of $100M***.

- Design problems at 0.13µm, which relate to lengthening times for bringing new products to market, continue to be extensive, specifically for designs that contain mixed-signal functionality, eg, high-speed I/O.

  Design capabilities are a competitive differentiation for most IC companies, especially as foundry supply is increasingly used. IDMs are increasing foundry supply because costs of establishing internal wafer fab capabilities are prohibitive, which makes design implementation a key competitive advantage.

- Many IC companies are encountering manufacturing yield problems with 0.13µm designs, which relates to link between design and process parameters.

  Yield problems with mixed-signal designs are more severe than for digital designs, and problems become more serious as feature dimensions shrink.

Yield problems are generally related to the need for IC product design limits to operate within process ranges, which requires designs to be extensively characterized.

- IC product costs (chip area), performance, power, etc, involve major trade-offs at timing closure. Necessary trade-offs to achieve timing closure can involve increased risks for design operations as complexity increases.

  Effective design tool use can be a major asset in obtaining timing closure, and training in use of EDA tools can help reduce risks.

- A key issue in IC design arena is how to bring IC designs to market within required time windows. Time-to-market is a critical competitive metric for most market segments.

  The difference in time-to-market capabilities of IC vendors generally relates to how effectively EDA tools are used, which includes training in use of tools as well as skill level of design engineers.

- IC functionality represents a key building block function in system design, and system design concepts must be increasingly addressed with migration to platform-level designs. IC vendors are migrating into systems architecture arena as well as providing chip set solutions, and design tools must support this trend.

- The total number of IC designs completed globally in 2004 will be flat or down, but design implementation costs will increase as complexity grows. There continue to be shortages of highly qualified IC design engineers.

Revenue per design will also need to increase in order to cover increased costs of implementing designs.

The ramp-up of 0.13µm and 90nm designs is slow due to implementation difficulties, but with indications that design problems at 0.13µm are starting to be addressed. Companies that have placed strong emphasis on design tools, training of design engineers, and a close link between design and process databases will be initially successful at 0.13µm.

- Embedding of processor engines and software customization are gaining momentum because design costs for IC products are growing rapidly.

  The trend is toward platform-level designs, ie, wireless handsets, DVD players, etc, which involves increased integration of software as well as providing platform-level capabilities.

  Software capabilities will increasingly complement hardware capabilities with the migration to platform-level designs, which requires the technology base within the IC industry to broaden.

  With the need to support increasing software demands, hardware design must become more efficient.

- Metal-programmable concepts, eg, RapidChip (LSI Logic) and ISSP (NEC), are likely to experience high growth because of low-cost prototypes and the ability to complete new designs within short time windows. New architectures are likely to emerge that can reduce design implementation costs within the structured ASIC environment.

- The programmable logic market, including conversion to structured ASIC designs, is showing growth because of the ability to bring new system designs to market within short time windows; however, there continue to be cost, performance, and power penalties associated with programmable logic concepts.

  Embedding of FPGA functionality with processors, etc, has growth potential due to the ability to support high performance and ease-of-customization for a range of applications.

- IC design implementation capabilities are building up in India, China, etc, due to the lower cost of engineers and the ability to hire many engineers.

  Design steps being implemented in China, India, etc, include functional as well as physical verification, and complete design projects will be done at these geographic locations in the future. Two to five years of training will be required to develop relatively strong design capabilities in China or India for high-complexity designs.

  Several large U.S. and European IC vendors are setting up design centers in China, India, etc, in order to access low-cost engineering resources.

- Design-for-yield optimization is becoming a key area of opportunity with the reduction in feature dimensions to 90nm. Design-for-yield optimization will need to address leakage issues, etc, and problems are expected to be severe for designs that try to minimize power dissipation and for designs that drive performance limits.

The IC industry is positioned for a turnaround, and IC vendors with strong design implementation capabilities will be the most successful in increasing market share and generating high profits as the market recovers.

Profits from the IC industry will be based on product leadership, competitive positioning, market environment, etc.

Design implementation capabilities are the key factor in enabling a strong competitive position to be established.

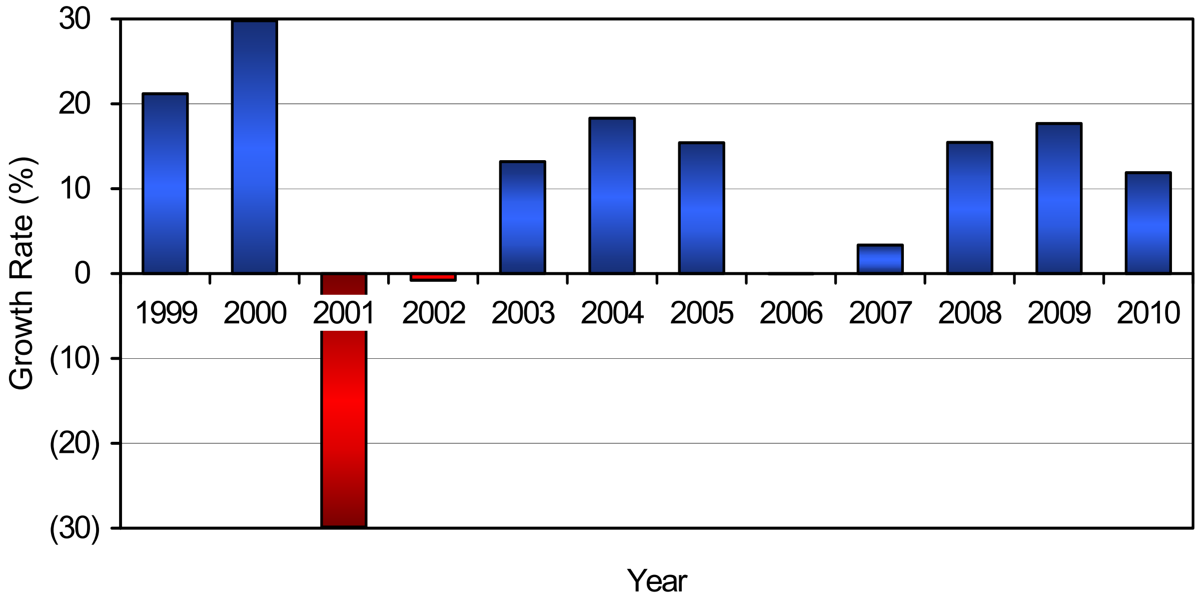
The key trends in the IC market by product category are shown in the following table.

TABLE 1
IC Market by Product Category

	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
MOS micro • Value ($M)	41,652	48,470	37,448	37,398	42,914	49,770	55,929	57,163	59,183	67,353	77,330	86,732
• Growth rate (%)	NA	16.37	(22.74)	(0.13)	14.75	15.98	12.37	2.21	3.53	13.80	14.81	12.16
• Percent total (%)	31.26	28.03	30.87	31.07	31.50	30.89	30.07	30.74	30.79	30.35	29.60	29.67
MPUs • Value ($M)	27,528	30,124	23,284	23,067	26,754	31,227	34,965	35,573	36,726	42,147	48,578	54,490
• Growth rate (%)	NA	9.43	(22.71)	(0.93)	15.98	16.72	11.97	1.74	3.24	14.76	15.26	12.17
• Percent total (%)	20.66	17.42	19.20	19.16	19.64	19.38	18.80	19.13	19.11	18.99	18.60	18.64
MCUs • Value ($M)	9,643	12,372	9,972	9,612	10,264	11,491	12,655	12,804	13,093	14,379	16,174	17,796
• Growth rate (%)	NA	28.30	(19.40)	(3.61)	6.78	11.95	10.13	1.18	2.26	9.82	12.48	10.03
• Percent total (%)	7.24	7.16	8.22	7.99	7.54	7.13	6.80	6.89	6.81	6.48	6.19	6.09
DSPs • Value ($M)	4,481	5,974	4,192	4,719	5,896	7,053	8,309	8,786	9,364	10,827	12,578	14,446
• Growth rate (%)	NA	33.32	(29.83)	12.57	24.95	19.61	17.82	5.73	6.58	15.63	16.17	14.85
• Percent total (%)	3.36	3.45	3.46	3.92	4.33	4.38	4.47	4.72	4.87	4.88	4.81	4.94
MOS logic • Value ($M)	35,718	46,299	35,396	32,354	35,559	41,097	48,118	48,039	48,498	54,110	61,851	68,388
• Growth rate (%)	NA	29.62	(23.55)	(8.59)	9.91	15.57	17.08	(0.16)	0.95	11.57	14.31	10.57
• Percent total (%)	26.81	26.78	29.18	26.88	26.11	25.50	25.87	25.83	25.23	24.38	23.68	23.40
Standard cell ASICs • Value ($M)	10,874	13,241	8,476	6,815	6,967	7,780	8,788	8,916	9,267	10,079	11,324	12,439
• Growth rate (%)	NA	21.77	(35.99)	(19.60)	2.23	11.67	12.95	1.46	3.94	8.76	12.35	9.85
• Percent total (%)	8.16	7.66	6.99	5.66	5.11	4.83	4.72	4.79	4.82	4.54	4.33	4.26
Gate array ASICs • Value ($M)	1,821	1,592	921	816	718	635	590	450	251	145	88	88
• Growth rate (%)	NA	(12.58)	(42.15)	(11.40)	(12.02)	(11.53)	(7.15)	(23.64)	(44.16)	(42.17)	(39.71)	NA
• Percent total (%)	1.37	0.92	0.76	0.68	0.53	0.39	0.32	0.24	0.13	0.07	0.03	0.03
Programmable logic • Value ($M)	2,684	4,127	2,592	2,357	2,676	3,190	3,832	4,160	4,593	5,361	6,360	7,274
• Growth rate (%)	NA	53.76	(37.19)	(9.07)	13.52	19.24	20.12	8.56	10.39	16.73	18.64	14.37
• Percent total (%)	2.01	2.39	2.14	1.96	1.96	1.98	2.06	2.24	2.39	2.42	2.43	2.49
MPR & special-purpose logic • Value ($M)	16,358	20,294	18,552	17,398	19,292	22,411	26,521	25,415	24,419	26,895	30,381	33,106
• Growth rate (%)	NA	24.06	(8.58)	(6.22)	10.88	16.17	18.34	(4.17)	(3.92)	10.14	12.96	8.97
• Percent total (%)	12.28	11.74	15.29	14.45	14.16	13.91	14.26	13.67	12.70	12.12	11.63	11.33
General-purpose logic • Value ($M)	1,807	2,939	1,649	1,339	1,446	1,609	1,836	1,779	1,703	1,817	1,960	2,061
• Growth rate (%)	NA	62.65	(43.89)	(18.80)	7.96	11.28	14.16	(3.12)	(4.27)	6.71	7.85	5.14
• Percent total (%)	1.36	1.70	1.36	1.11	1.06	1.00	0.99	0.96	0.89	0.82	0.75	0.71
Display drivers • Value ($M)	2,174	4,106	3,206	3,629	4,461	5,472	6,551	7,318	8,265	9,812	11,739	13,420
• Growth rate (%)	NA	88.87	(21.92)	13.19	22.94	22.65	19.71	11.72	12.93	18.73	19.63	14.32
• Percent total (%)	1.63	2.37	2.64	3.01	3.28	3.40	3.52	3.94	4.30	4.42	4.49	4.59
Analog • Value ($M)	21,359	29,982	23,207	23,921	26,498	30,960	35,719	37,641	39,963	45,326	51,803	57,434
• Growth rate (%)	NA	40.37	(22.60)	3.08	10.77	16.84	15.37	5.38	6.17	13.42	14.29	10.87
• Percent total (%)	16.03	17.34	19.13	19.87	19.45	19.21	19.20	20.24	20.79	20.42	19.83	19.65
MOS memory • Value ($M)	34,503	48,163	25,251	26,694	31,244	39,314	46,237	43,107	44,581	55,164	70,252	79,750
• Growth rate (%)	NA	39.59	(47.57)	5.71	17.04	25.83	17.61	(6.77)	3.42	23.74	27.35	13.52
• Percent total (%)	25.90	27.85	20.82	22.18	22.94	24.40	24.86	23.18	23.19	24.85	26.89	27.28
TOTAL IC value ($M)	133,232	172,914	121,302	120,367	136,215	161,142	186,003	185,949	192,225	221,954	261,236	292,303
• Growth rate (%)	NA	29.78	(29.85)	(0.77)	13.17	18.30	15.43	(0.03)	3.37	15.47	17.70	11.89

The IC market will continue to cycle, as shown in the following figure.

FIGURE 1
IC Market by Product Category



The cycling of the IC market is due to changes in demand within high-value end markets as well as to oversupply and shortage situations.

The issues in the IC market include:.

- The IC market is entering a growth phase, with the next downturn probably in 2006. The growth of the IC market in 2005 will be driven by continued strength of the U.S. economy.

- The IC market by product category represents a traditional reporting structure of the IC industry. IC vendors also generate revenues from products.

- The growth in revenues of products such as DSPs is based on increasing product volumes as well as on increased integration levels of products. As functions such as co-processors are integrated with DSPs, the value of end-products increases.

The growth of the IC market will stimulate more design activity for new products.

The IC market by application segment is shown in the following table.

TABLE 2
IC Market by Application Segment

	1999	2000	2001	2002	2003	2004	2005	2006	2007
Computer system Value ($M)	52,742	64,602	42,401	42,808	47,662	56,432	65,640	65,380	68,836
Growth rate (%)	NA	22.49	(34.37)	0.96	11.34	18.40	16.32	(0.40)	5.29
Percent total (%)	39.59	37.36	34.95	35.56	34.99	35.02	35.29	35.16	35.81
Computer peripheral Value ($M)	11,605	14,891	11,482	11,403	12,968	15,180	16,722	16,345	16,666
Growth rate (%)	NA	28.31	(22.89)	(0.69)	13.72	17.06	10.16	(2.25)	1.96
Percent total (%)	8.71	8.61	9.47	9.47	9.52	9.42	8.99	8.79	8.67
Wireline communications Value ($M)	16,983	25,290	13,879	10,853	10,107	10,780	12,239	13,407	15,705
Growth rate (%)	NA	48.92	(45.12)	(21.80)	(6.87)	6.66	13.53	9.54	17.14
Percent total (%)	12.75	14.63	11.44	9.02	7.42	6.69	6.58	7.21	8.17
Wireless communications Value ($M)	20,826	25,754	17,864	18,382	22,966	28,377	33,276	33,508	32,486
Growth rate (%)	NA	23.66	(30.63)	2.90	24.94	23.56	17.26	0.70	(3.05)
Percent total (%)	15.63	14.89	14.73	15.27	16.86	17.61	17.89	18.02	16.90
Consumer Value ($M)	21,289	29,714	24,427	25,263	29,586	35,886	42,111	41,485	41,943
Growth rate (%)	NA	39.57	(17.79)	3.42	17.11	21.30	17.35	(1.49)	1.10
Percent total (%)	15.98	17.18	20.14	20.99	21.72	22.27	22.64	22.31	21.82
Other Value ($M)	9,787	12,663	11,249	11,657	12,927	14,487	16,015	15,824	16,589
Growth rate (%)	NA	29.39	(11.17)	3.63	10.89	12.07	10.55	(1.19)	4.83
Percent total (%)	7.35	7.32	9.27	9.68	9.49	8.99	8.61	8.51	8.63
TOTAL Value ($M)	133,232	172,914	121,302	120,367	136,215	161,142	186,003	185,949	192,225
Growth rate (%)	NA	29.78	(29.85)	(0.77)	13.17	18.30	15.43	(0.03)	3.37

The issues in the IC market by application segment include:

- Wireless communications applications show the highest growth due to the increase in the volume of wireless handsets and the greater functionality of IC products.

  As wireless handsets add more and more features, IC complexity increases.

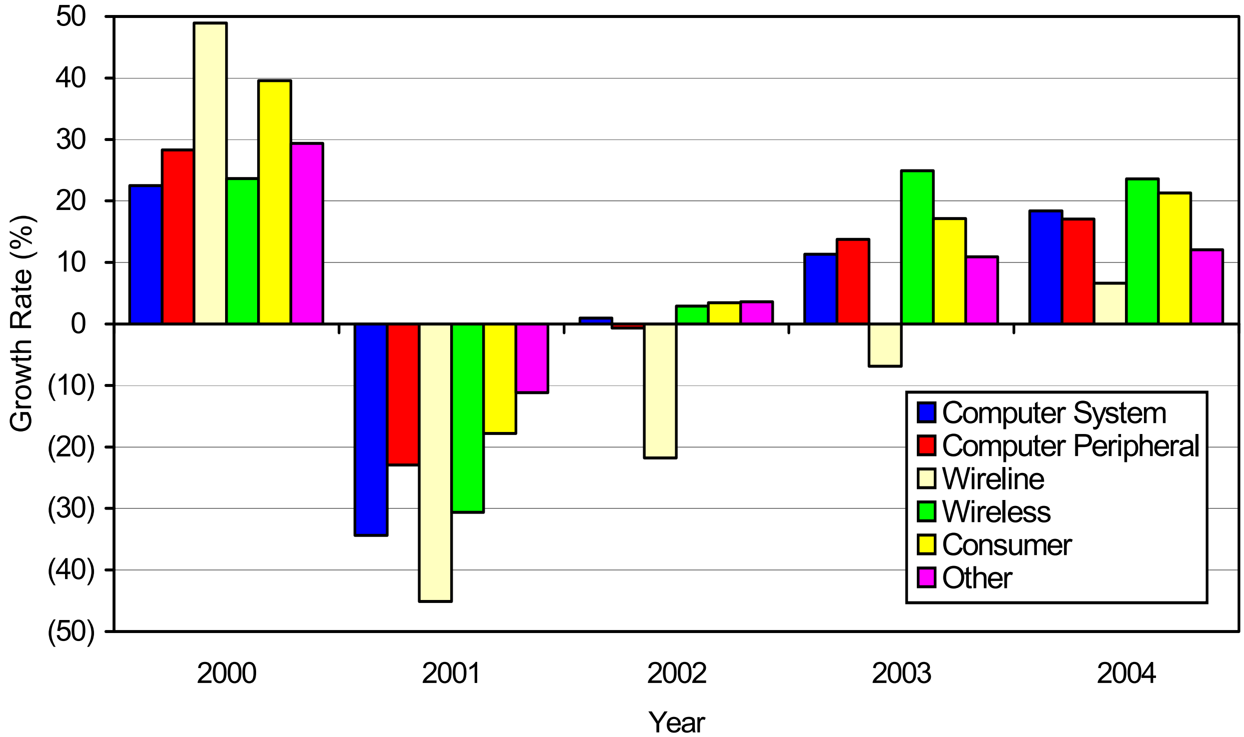
- Consumer applications show high growth, with products such as high-definition televisions, recordable DVD players, and digital cameras showing high growth. The complexity of IC designs in the consumer market, such as for game consoles, is showing a large increase.

  Consumer is a key driver for the combination of high performance and low cost.

The IC market is becoming increasingly application-specific, with the need for specialized IP for various end-market segments.

A perspective on the cycling of the IC market by application segment is shown in the following figure.

FIGURE 2
IC Market by Application Segment



The growth of the IC market is application-specific, with increased specialization within various geographic regions.

A perspective on the IC market by geographic region is shown in the following table.

TABLE 3
IC Market by Geographic Region

	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
North America																
IC ($M)	43,178	38,247	41,924	37,708	43,701	53,894	32,951	29,264	29,498	32,978	36,215	34,921	35,196	39,819	46,187	50,188
• Growth rate (%)	NA	(11.42)	9.61	(10.06)	15.89	23.32	(38.86)	(11.19)	0.80	11.80	9.81	(3.57)	0.79	13.13	15.99	8.66
• Percent WW (%)	34.92	33.83	35.28	34.29	32.80	31.17	27.16	24.31	21.66	20.47	19.47	18.78	18.31	17.94	17.68	17.17
Japan																
IC ($M)	32,894	27,153	26,175	21,063	27,162	36,182	27,165	24,986	29,847	33,871	36,550	35,349	35,850	40,640	46,892	50,919
• Growth rate (%)	NA	(17.45)	(3.60)	(19.53)	28.96	33.21	(24.92)	(8.02)	19.45	13.48	7.91	(3.28)	1.42	13.36	15.38	8.59
• Percent WW (%)	26.60	24.02	22.03	19.16	20.39	20.92	22.39	20.76	21.91	21.02	19.65	19.01	18.65	18.31	17.95	17.42
Europe																
IC ($M)	24,507	23,058	25,505	25,524	27,961	35,924	25,671	24,195	26,985	29,852	33,071	31,370	31,256	35,579	40,544	44,810
• Growth rate (%)	NA	(5.91)	10.61	0.07	9.55	28.48	(28.54)	(5.75)	11.53	10.62	10.78	(5.15)	(0.36)	13.83	13.95	10.52
• Percent WW (%)	19.82	20.40	21.46	23.21	20.99	20.78	21.16	20.10	19.81	18.53	17.78	16.87	16.26	16.03	15.52	15.33
ROW																
IC ($M)	23,061	24,585	25,223	25,659	34,408	46,914	35,515	41,922	49,885	64,441	80,167	84,309	89,923	105,916	127,614	146,385
• Growth rate (%)	NA	6.61	2.60	1.73	34.10	36.35	(24.30)	18.04	18.99	29.18	24.40	5.17	6.66	17.79	20.49	14.71
• Percent WW (%)	18.65	21.75	21.23	23.34	25.83	27.13	29.28	34.83	36.62	39.99	43.10	45.34	46.78	47.72	48.85	50.08
Worldwide																
IC ($M)	123,640	113,043	118,827	109,954	133,232	172,914	121,302	120,367	136,215	161,142	186,003	185,949	192,225	221,954	261,236	292,303
• Growth rate (%)	NA	(8.57)	5.12	(7.47)	21.17	29.78	(29.85)	(0.77)	13.17	18.30	15.43	(0.03)	3.37	15.47	17.70	11.89

The issues regarding the IC market by geographic region include:

- ROW, which is primarily the Far East, increases from 19 percent in 1995 to 50 percent of the total IC market in 2010. There is continued growth of contract manufacturing as well as increasing design activity for ICs and systems in the Far East.

  The design environment will need to address changing geographic composition of the IC market.

- North American, European, and Japanese markets continue to drive new technology concepts. Consequently, strong design implementation capabilities must be established in order to address complex segments of the IC market.

Yearly changes in the IC market are not significant, but changes from a five- or ten-year perspective are major.

The IC market is becoming increasingly processor-specific, which is shown in the following figures.

FIGURE 3a
IC Market by Product Category

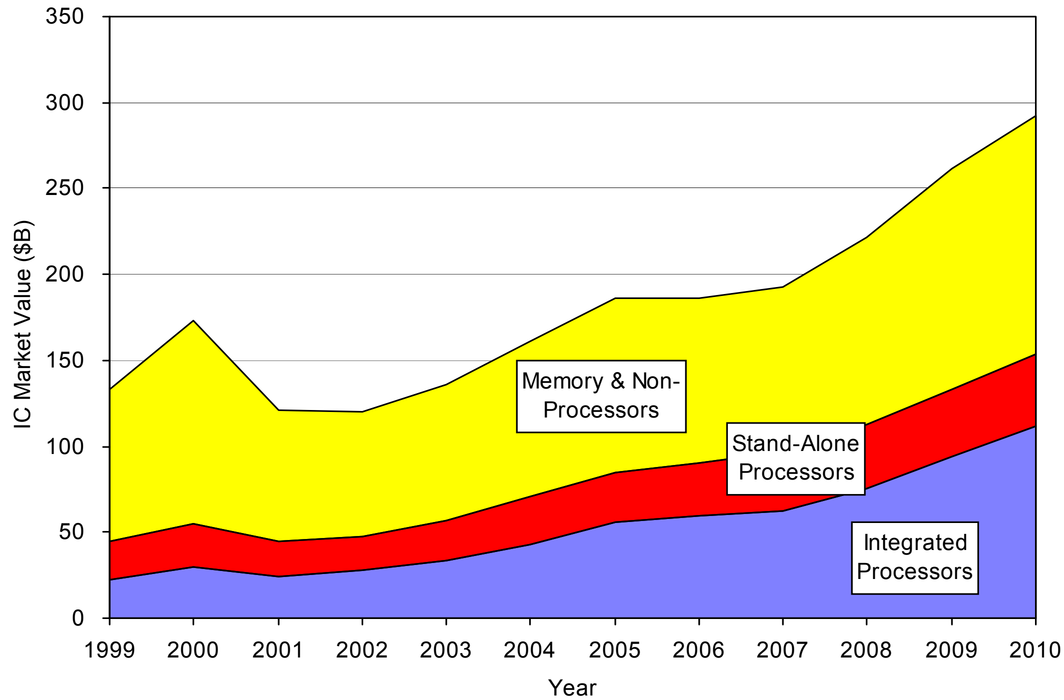
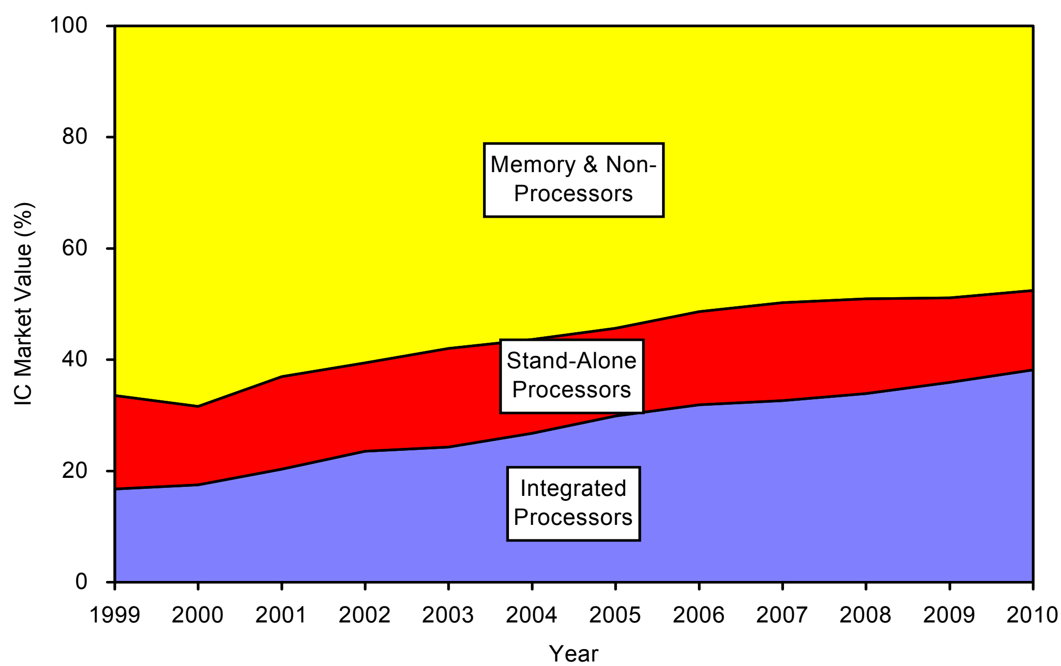


FIGURE 3b
IC Market by Product Category



The issues regarding revenue segmentation of the IC industry include:

- Processor revenues are segmented into stand-alone, such as supplied by Intel, AMD, etc, and embedded processor cores, which are included in products such as wireless handset baseband functionality.

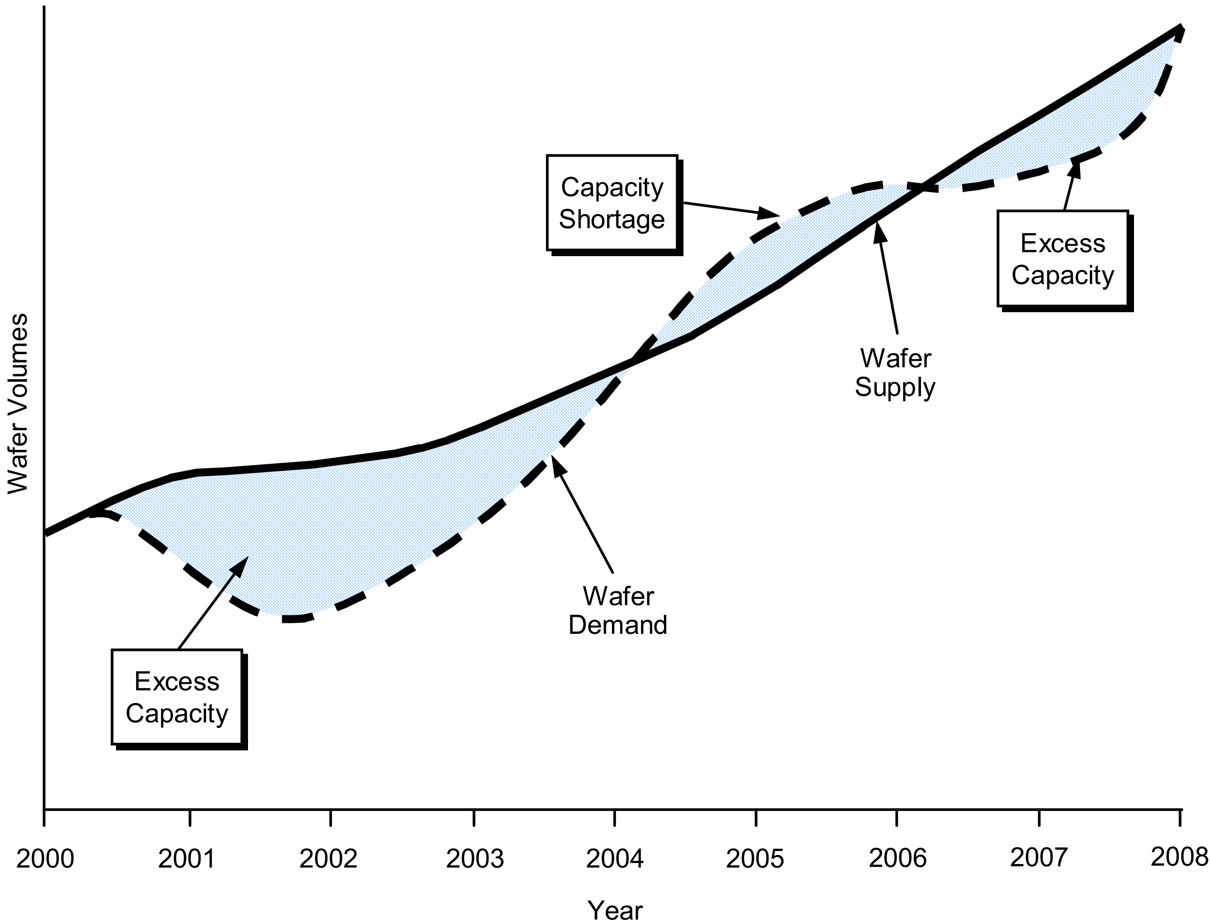
- Design capabilities will increasingly need to address processor-based designs, which can involve integration of hard and soft cores.

  The software base of the IC industry will build on the processor base.

A wide range of processor types will be integrated, with the emergence of application-specific processor architectures.

The IC industry is in a capacity shortage phase, as shown in the following figure.

FIGURE 4
Wafer Supply/Demand Environment



The issues regarding the supply/demand phase of the IC industry include:.

- The shortage phase of the IC industry is expected to last two years (end of 2005).

  With large commitments to expand wafer manufacturing capacity, there will likely be overcapacity in advanced features (90nm and 0.13μm) in late 2005.

- The industry cycling is expected to continue, but costs of having excess wafer fab capacity can be huge at 90nm (depreciation of wafer fab can be $600M per year). Consequently, relatively few IC vendors worldwide will be able to commit to 65nm capacity.

The IC industry is currently in a growth phase, and capacity shortages are emerging. There will be intense pressures to increase design productivity in order to broaden the product base of IC vendors. Also, in order to optimize output from wafer fab facilities, it is important to implement new product designs with smaller chip areas, etc.

As the industry enters a down phase, it is important to stimulate product design activity in order to develop new applications, which can result in the future recovery of the IC market.

The analysis of the IC vendor financial performance shows large performance differences during the downturn of the IC market.

The financial performance of selected IC vendors (publicly traded) is shown in the following table.

TABLE 4
Financial Performance of Selected IC Vendors (CY)

IC vendor	CY 2000					CY 2001					CY 2002					CY 2003				
	Rev $M	R&D exp		Net income		Rev $M	R&D exp		Net income		Rev $M	R&D exp		Net income		Rev $M	R&D exp		Net income	
		$M	%	$M	%		$M	%	$M	%		$M	%	$M	%		$M	%	$M	%
Actel	226	37	16.2	41	18.3	146	38	26.2	(5)	(3.2)	134	39	29.3	0.1	0.1	150	40	26.4	6	4.2
Agere Systems(**)(***)	5,104	930	18.2	(174)	(3.4)	3,255	869	26.7	(4,987)	(153.2)	2,038	613	30.1	(1,582)	(77.6)	1,919	453	23.6	(256)	(13.3)
Altera	1,377	172	12.5	497	36.1	839	171	20.4	(40)	(4.7)	712	183	25.7	91	12.8	827	179	21.6	155	18.8
AMCC	372	75	20.1	(221)	(59.6)	244	156	64.1	(3,709)	(1,521)	112	139	124.1	(607)	(543.6)	104	116	111.8	(332)	(319.3)
AMD	4,644	642	13.8	983	21.2	3,892	651	16.7	(61)	(1.6)	2,697	816	30.3	(1,303)	(48.3)	3,519	852	24.2	(274)	(7.8)
Analog Devices(*)(**)	3,049	459	15.1	768	25.2	1,898	448	23.6	191	10.0	1,782	523	29.4	141	7.9	2,106	447	21.2	318	15.1
ATI*	1,309	143	10.9	(139)	(10.6)	946	152	16.1	(48)	(5.1)	1,091	173	15.9	(32)	(3.0)	1,511	228	15.1	74	4.9
Atmel	2,013	252	12.5	266	13.2	1,472	268	18.2	(418)	(28.4)	1,194	253	21.2	(642)	(53.8)	1,331	248	18.6	(118)	(8.9)
Broadcom	1,096	251	22.9	(688)	(62.7)	962	447	46.4	(2,742)	(285.1)	1,083	462	42.6	(2,237)	(206.5)	1,610	434	27.0	(960)	(59.6)
Conexant	2,004	445	22.2	(442)	(22.1)	839	449	53.5	(1,450)	(172.8)	605	285	47.1	(1,126)	(186.2)	633	158	25.0	(39)	(6.2)
Cypress	1,288	184	14.3	277	21.5	819	268	32.7	(407)	(49.7)	775	250	32.2	(249)	(32.2)	837	239	28.5	(5)	(0.6)
ESS Technology**	303	28	9.2	63	20.8	271	28	10.3	11	4.0	273	27	9.9	37	13.6	150	32	21.1	22	14.7
Fairchild	1,781	84	4.7	273	15.3	1,408	83	5.9	(42)	(3.0)	1,412	82	5.8	(3)	(0.2)	1,396	75	5.4	(82)	(5.8)
Infineon	7,975	1,169	14.7	1,386	17.4	5,667	1,359	24.0	(1,358)	(24.0)	5,521	1,092	19.8	(751)	(13.6)	7,400	1,285	17.4	(391)	(5.3)
Intel	33,726	3,897	11.6	10,535	31.2	26,539	3,796	14.3	1,291	4.9	26,764	4,034	15.1	3,117	11.6	30,141	4,360	14.5	5,641	18.7
Intersil	713	103	14.4	64	8.9	576	128	22.3	49	8.5	420	78	18.6	(5)	(1.2)	508	91	18.0	46	9.0
Lattice**	568	77	13.6	168	29.6	295	72	24.3	(110)	(37.1)	229	86	37.4	(175)	(76.5)	223	86	38.6	(77)	(34.4)
Linear Tech	887	92	10.4	408	46.1	723	90	12.5	302	41.7	558	86	15.4	216	38.8	680	96	14.2	270	39.8
LSI Logic	2,738	379	13.8	237	8.6	1,785	503	28.2	(992)	(55.6)	1,817	457	25.2	(292)	(16.1)	1,693	433	25.6	(309)	(18.2)
Marvell(*)(**)	144	35	24.4	(235)	(163.4)	289	93	32.3	(415)	(143.8)	505	146	28.8	(72)	(14.3)	769	205	26.7	34	4.5
Maxim**	1,477	240	16.3	422	28.6	1,203	277	23.0	218	18.1	1,111	279	25.2	286	25.7	1,189	272	22.9	329	27.7
Micron*	6,590	475	7.2	1,515	23.0	2,788	505	18.1	(1,243)	(44.6)	2,850	561	19.7	(957)	(33.6)	3,513	688	19.6	(956)	(27.2)
National*	2,380	402	16.9	733	30.8	1,583	439	27.8	(116)	(7.3)	1,632	439	26.9	(13)	(0.8)	1,728	393	22.8	55	3.2
NEC Electronics(*)(**)	6,615	806	12.2	360	5.4	5,160	752	14.6	(401)	(7.8)	6,145	819	13.3	82	1.3	6,365	908	14.3	250	3.9
NVIDIA(*)(**)(****)	735	86	11.8	100	13.6	1,369	155	11.3	177	12.9	1,909	225	11.8	91	4.8	1,801	264	14.7	67	3.7
PMC-Sierra	695	179	25.7	75	10.8	323	201	62.3	(639)	(198.0)	218	138	63.2	(65)	(29.8)	249	119	47.9	(8)	(3.2)
SanDisk	602	46	7.7	299	49.6	366	59	16.1	(298)	(81.3)	541	63	11.7	36	6.7	1,080	84	7.8	169	15.6
STMicro	7,813	1,026	13.1	1,452	18.6	6,357	978	15.4	257	4.0	6,318	1,022	16.2	429	6.8	7,238	1,238	17.1	253	3.5
TI	11,875	1,747	14.7	3,058	25.8	8,201	1,598	19.5	(201)	(2.5)	8,383	1,619	19.3	(344)	(4.1)	9,834	1,748	17.8	1,198	12.2
TSMC	5,328	164	3.1	2,087	39.2	3,725	315	8.5	429	11.5	4,654	339	7.3	625	13.4	5,865	369	6.3	1,373	23.4
UMC	3,183	180	5.7	1,538	48.3	1,843	245	13.3	(90)	(4.9)	1,939	202	10.4	203	10.5	2,498	168	6.7	413	16.5
Vitesse	517	105	20.3	55	10.6	258	167	64.7	(247)	(95.6)	156	147	93.7	(788)	(503.6)	171	110	64.2	(164)	(96.0)
Xilinx	1,559	188	12.0	674	43.2	1,149	204	17.7	(310)	(27.0)	1,124	215	19.2	111	9.8	1,300	242	18.6	222	17.0
TOTAL IC Vendor	120,686	15,096	12.5	26,433	21.9	87,190	15,965	18.3	(17,406)	(20.0)	86,701	15,892	18.3	(5,778)	(6.7)	100,338	16,660	16.6	6,923	6.9
TOTAL IC Market	172,914	--	--	--	--	121,302	--	--	--	--	120,367	--	--	--	--	136,215	--	--	--	--
Percent IC Market	69.8	--	--	--	--	71.9	--	--	--	--	72.0	--	--	--	--	73.7	--	--	--	--

Note:
* CYs for Analog Devices (FY ends Oct), Marvell (FY ends Jan), and NVIDIA (FY ends Jan) reflect Feb-Jan; CYs for ATI (FY ends Aug), Micron (FY ends Aug), and National (FY ends May) reflect Dec-Nov; CYs for NEC Electronics (FY ends Mar) reflect Apr-Mar.
** Annualized 2003.
*** 1996 through 1999 figures reflect revenues of Lucent Technologies' microelectronics business.
**** CY98 reflects Jan 1, 1998 through Jan 31, 1999 due to change in FY.

The analysis of the financial performance of selected IC vendors includes:

- The companies that are analyzed represent approximately 70 percent of the IC market. As the spin-off of vertically integrated organizations increases, eg, Motorola SPS, this percentage will increase.

- IC vendors' net incomes totaled $26.4B in 2000, but cumulative losses were $17.4B in 2001 and $5.8B in 2002, and profits were $6.9B in 2003. Profits are expected to be significantly higher in 2004 than in 2003 (some vendors, such as Intel, STMicroelectronics, Linear Technology, Maxim, TSMC, and NVIDIA, were able to generate profits during the downturn).

Profitable companies were able to establish product technology leadership within targeted market segments, which relates to design capability leadership.

The key trend in the IC industry is increasing R&D expenditures, which have shown significant growth from the mid-1990s through 2003.

The R&D expenditures of selected semiconductor vendors (17 percent of IC market in 2003) in value and as a percentage of revenues are shown in the following figures.

FIGURE 5a
R&D Expenditures of Selected IC Vendors

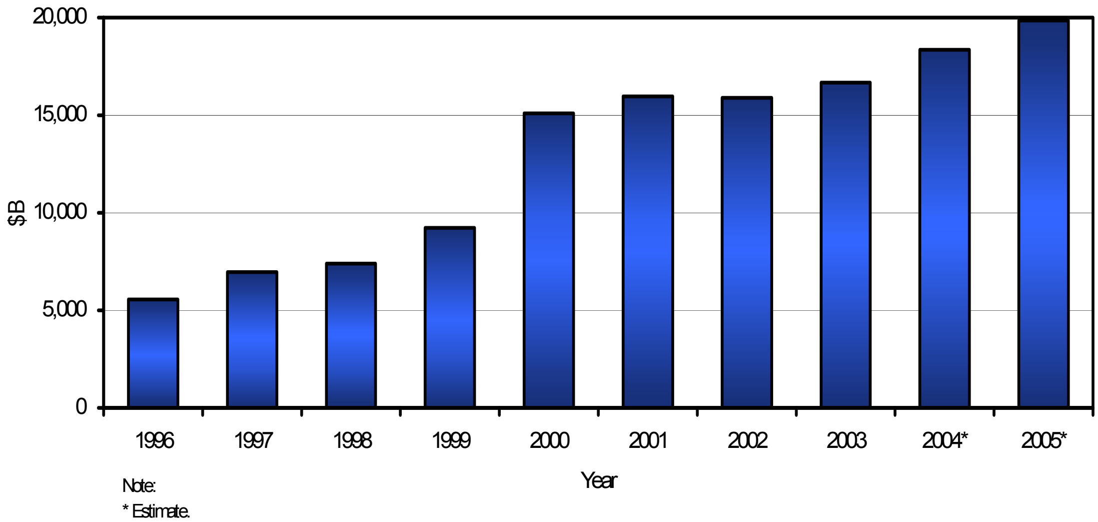
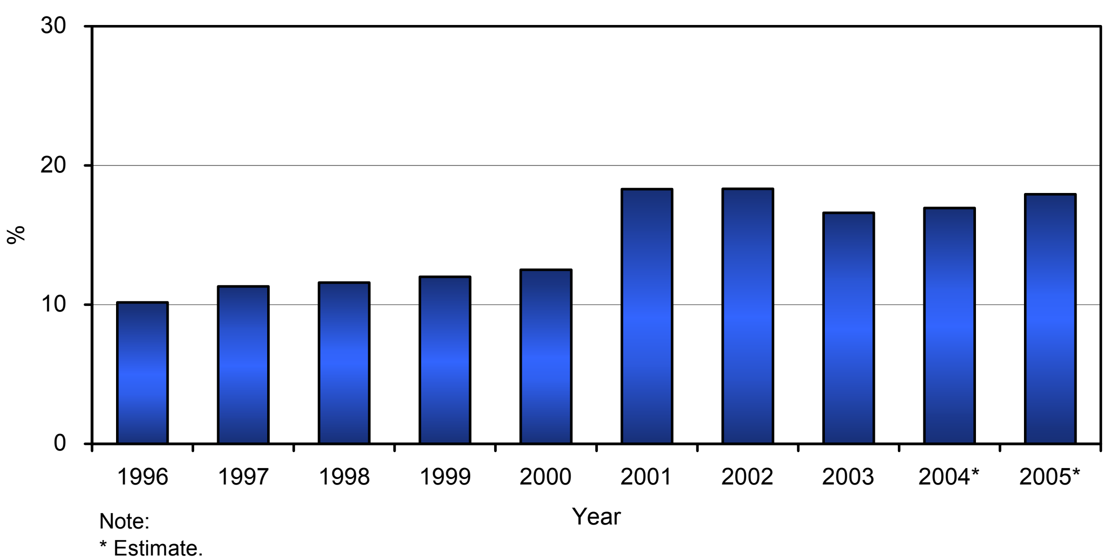


FIGURE 5b
R&D Expenditures (as Percentage of Revenues) of Selected IC Vendors



The issues regarding R&D expenditures include:

- R&D expenditures have increased from 10 percent of revenues in the mid-1990s to 15 to 20 percent of revenues in 2003 for IC vendors. R&D expenditures will likely be at 20+ percent of revenues for platform-level IC vendors.

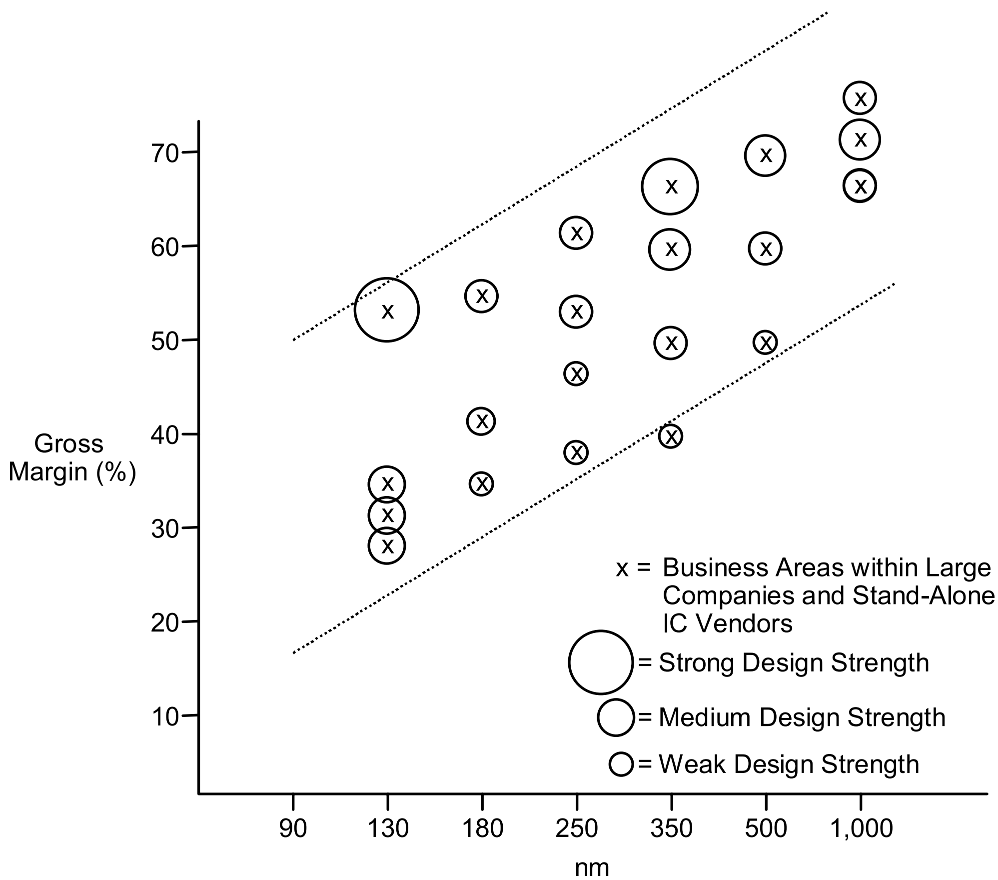
- EDA tool expenditures are tied to R&D expenditures; however, the EDA market has not shown the same increase as R&D expenditures of IC vendors.

  EDA spending has declined as a percentage of the R&D budget, which has led to the present design crisis. However, IC vendors that show strong financial performance have ensured leadership design implementation capabilities within targeted business areas and market segments.

- Profits (gross margins) of IC vendors are linked to design strengths (which are based on customer inputs) for ASSPs and ASICs.

  There is a direct correlation between design capabilities and gross margins, and trends in this arena are shown in the following figure.

FIGURE 6
Gross Margin Design Strength per Feature Dimension



IC vendors, such as Maxim, and the IC business units of large IC vendors, such as the mixed-signal business units of TI and STMicroelectronics, that have lagging feature dimensions generally have higher gross margins than IC vendors or business units that drive advanced feature technologies (Intel is an exception).

There has been a selection process within IC companies in mature or lagging feature dimensions based on design capabilities, ie, weak companies have abandoned the market.

Also, design productivity and design capabilities have not tracked the feature dimension enhancements and the increase in design complexity.

Analysis shows that within some large IDMs, gross margins for high-complexity advanced feature digital designs can be less than 30 percent, while gross margins for mixed-signal designs within the same companies can be 50 to 60 percent. This type of gross margin difference can be partly attributed to the learning phase associated with advanced feature digital designs but is also associated with the high design skill level required for mixed-signal designs in lagging features. R&D expenditures for advanced high-complexity products within these companies can exceed 20 percent, while R&D for mature products can be 10 to 12 percent of revenues.

The analysis of gross margins of publicly traded companies (based on various product groups and business units within these companies) also shows that R&D expenditures are higher for designs with advanced features (as percentage of revenues) than for lagging feature dimension designs.

The analysis of gross margin levels shows that it is not feature dimensions but design implementation capabilities that represent the basis for generating high gross margins.

Low gross margins and high product development costs of advanced feature IC designs are key indicators that the global IC industry must dramatically increase design engineering productivity.

It is significant that for companies in products such as programmable logic, gross margins for designs that have mature feature dimensions are higher than those for advanced feature products.

- The design strengths of IC vendors are related to:.

  - EDA tool expenditures. While EDA tool expenditures are based on the negotiating skills of IC vendors, there are minimum expenditures required to build the design capabilities base.

  - Training in use of tools. Training in use of design tools represents a key factor in the productivity of design teams, especially as designs become increasingly complex (which necessitates that performance and capabilities of design tools be optimized).

  - Emphasis by top management on design capabilities. This relates to the perceived role of design implementation capabilities in the competitiveness of IC vendors and the willingness of top management to commit to leadership design implementation capabilities.

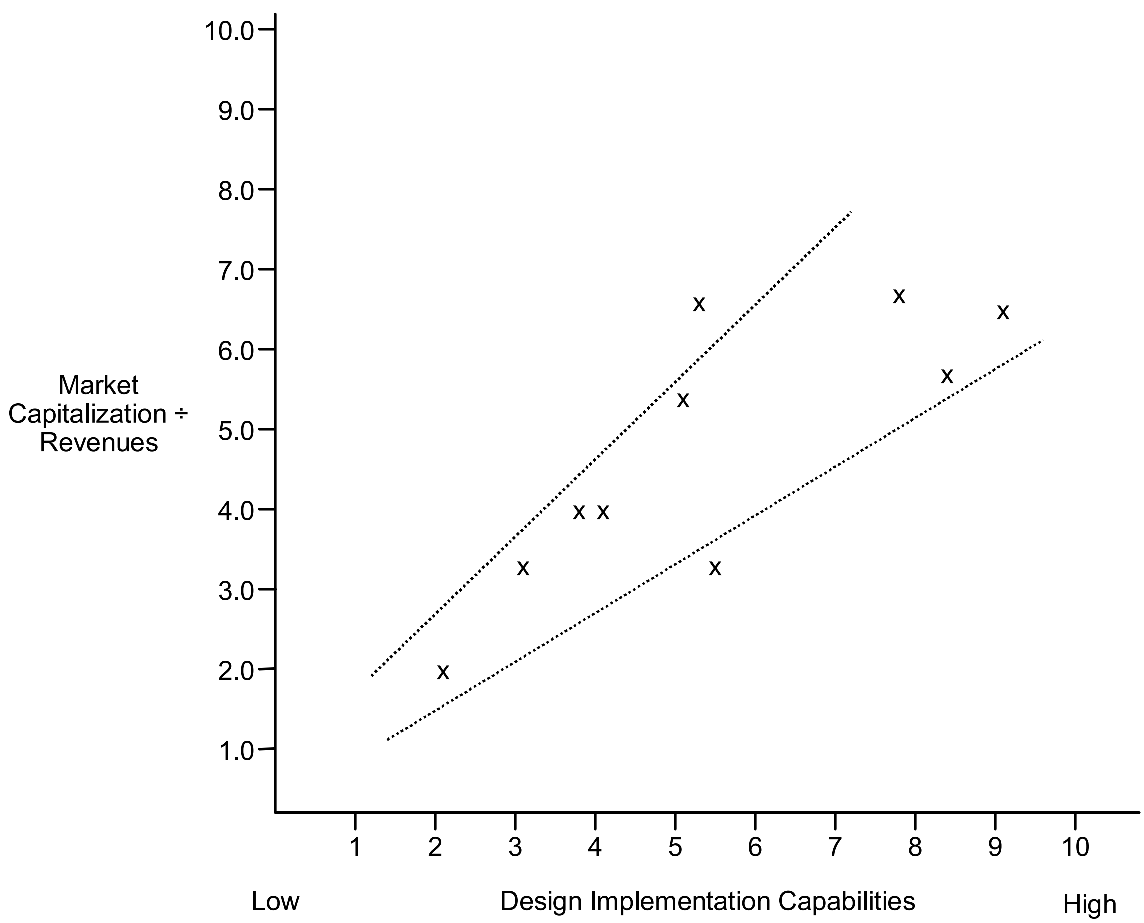
    Some IC vendors have adopted the strategy of considering manufacturing as a competitive advantage and therefore place relatively little emphasis on design implementation capabilities.

Design strengths are relative, and assessment of capabilities in this arena is based on the product portfolio of IC vendors as well as on inputs from their customers. The analysis of various design projects also helps to determine the effectiveness of IC vendors in bringing complex new IC products to market.

- The analysis of competitive positioning and market capitalization of IC vendors (returns for shareholders) relates to profits, which in turn relate to strengths in the design arena.

  Design implementation capabilities of IC vendors (compared to market capitalization divided by revenues) are illustrated in the following figure.

FIGURE 7
Design Implementation Comparison (y-axis unit of measure $B?)



The issues regarding the value of IC vendors based on their design implementation capabilities include:

- Market capitalization (share price multiplied by number of shares) divided by revenues provides a perspective on the relative value of companies as perceived by shareholders.

- Design implementation capabilities are an assessment of relative strengths of IC vendors (10 high) based on customer input, product capabilities, etc.

The analysis shows a close link between financial performance metrics of IC vendors and their design implementation capabilities.

Other factors, such as IP and consistency of management in implementing strategies, impact market valuation of IC vendors, but strong design implementation is a requirement for profits, regardless of technology feature dimension.

IC companies that have strong design implementation capabilities continue to have high market capitalization. This type of environment is linked to profit premiums that are obtained from design leadership and the ability for new products to be effectively positioned in the market.

The EDA industry and IC design environment have historically operated with multiple technical skill sets. ***Although rigorous technical disciplines are still important, in order to obtain more funding for addressing design implementation limitations, decision processes must be elevated to financial metrics***. Top management of the IC industry is motivated by financial returns and by how to improve financial performance. If there is broad-based acceptance within the IC industry that market valuation of IC vendors is directly related to design implementation capabilities (other capabilities are also important), there can be increased emphasis on improving design implementation capabilities for highly complex advanced feature designs.

The IC vendor rankings of relative importance of design factors at 0.13μm are shown in the following table.

TABLE 5
Customer Rankings of Design Factors at 0.13μm (10 High)

Factor	Ranking	Comments
Utilizing installed base of EDA tools and databases	9.9	All companies (except new ones) want to continue using installed base of design expertise and databases
Time-to-market	9.5	All IC companies consider on-time IC design completion critical, but with different time-to-market metrics by application segment
IC design operating as expected	9.0	Operating as expected can be defined as either meeting specification or IC operating in end system
Minimizing chip area	6.8 to 8.9	Importance is determined by end market being addressed and time-to-market competitive pressures Can compromise by taking longer to complete designs
Driving performance limits	4.9 to 9.1	Depends on market segment being addressed For many application segments, performance challenges with 0.13μm designs are low
Meeting power budgets	4.7 to 9.0	Power is major challenge for portable applications and very high-performance designs
Integrating IP and IP interface efficiently	7.5 to 8.8	Important for most IC vendors. Includes qualification of IP Impacts time-to-market for designs
Migrating to next-generation technology	2.6 to 5.4	Some companies consider it attractive to migrate to next-generation technology, but emphasis within mainstream design environment is on addressing current projects
System-level design concepts	2.9 to 4.9	Research organizations are very interested in system-level concepts, but design project teams are focused on IC design
Co-developing hardware and software	3.1 to 4.7	IC design project teams are not very interested in co-developing hardware and software because skills are mostly in IC design Research organizations are very interested in next-generation concepts

The issues regarding customer inputs include:

- Customers are highly motivated to maintain and strengthen their existing base of design capabilities. Incremental enhancements in capabilities must be made based on new design tools, etc.

- Design tool capabilities must correspond with the short-term needs of customers, which is to make design project teams successful. Although the IC industry is oriented towards long-term success, priorities are often placed on bringing new products to market within short time windows.

- R&D organizations are interested in system-level concepts, software issues, etc, but in many cases, budgets are low.

Future requirements of design concepts need to be balanced against the short-term needs of quickly bringing new IC designs to market.

IC vendor inputs on design factors at 0.13μm are shown in the following table.

TABLE 6
Design Factors at 0.13µm

Design Factors	Comments
90 percent of designs are renditions of previous designs	Represents continuation of past patterns because cost of implementing new architectures is very high
50+ percent of design engineers' time is spent on functional verification	Functional verification requirements tie into problems with timing closure as well as into logic issues By establishing stringent design disciplines, time required for functional verification can be reduced, albeit with some potential chip area and performance penalties
80+ percent of logic gates are for embedded IP	IP availability and qualification can be key factors in completing designs on time Most important embedded IP is processor cores
Interconnect delays and parasitics dominate performance of high-speed critical paths	Need close link between physical design steps and synthesis as well as tight tolerances on interconnect structures Predictive capabilities for interconnect parasitics are used early in design process and need to be enhanced
Power budgets are becoming as important for many designs as chip area budgets	Ability to predict power budgets early on in design process is becoming increasingly important, and tools for doing so need to be enhanced
Platform-level design is becoming increasingly important	Present approach is to have separate design effort for IC products (sold as stand-alone products) and platform-level solutions (where software dominates) Co-developing IC products and platforms is conceptually attractive, but design disciplines are very different
ESL concept is attractive, but its use has been limited to date	Skill level and design disciplines needed for IC design and system design differ, and bridge capability is required New tools are needed that tie system design to IC design

A perspective on the design environment includes:

- Design tools need to correspond with design engineering activities, and budgets of CAD organizations are related to addressing short-term problems. There also continue to be intense pressures to reduce EDA licensing expenditures among all IC vendors.

- Time-to-market for new IC designs is lengthening, even with an increase in the head count of design teams.

Equipment vendor design times are shortening, and product life cycles in areas such as consumer can last six to nine months.

Time-to-market requirements necessitate significant enhancements in design productivity.

- Chip area for many designs is larger than expected at 0.13µm, which increases costs and slows migration to new technology nodes.

- IC product yields for many 0.13µm designs are not at expected levels. Yield problems can be even more severe at 90nm because of increase in impact of parasitics.

- Leakage components are becoming critical for IC performance at 0.13µm and will be a major problem at 90nm. Methods to address this problem include use of higher voltages, SOI, etc. Design expertise is also critical to reduce impact of leakage, etc, problems.

- Power consumption is too high for many designs and represents key problem for many system designs.

- Performance distribution of IC products is not satisfactory for many high-speed and processor designs, which reduces revenue potential.

- Growth of 0.13µm designs (and potentially of IC industry) is being impacted by skill base in using EDA tools. Problems will be more serious at 90nm.

  EDA tool performance is strongly impacted by the level of training of design engineers.

The problems in IC design at 0.13µm and 90nm represent a major opportunity for the EDA industry if appropriate approaches are established to address design problems.

- The market for EDA tools is positioned for accelerating growth in 2004 and 2005 due to the recovery of the IC market and an increase in R&D spending.

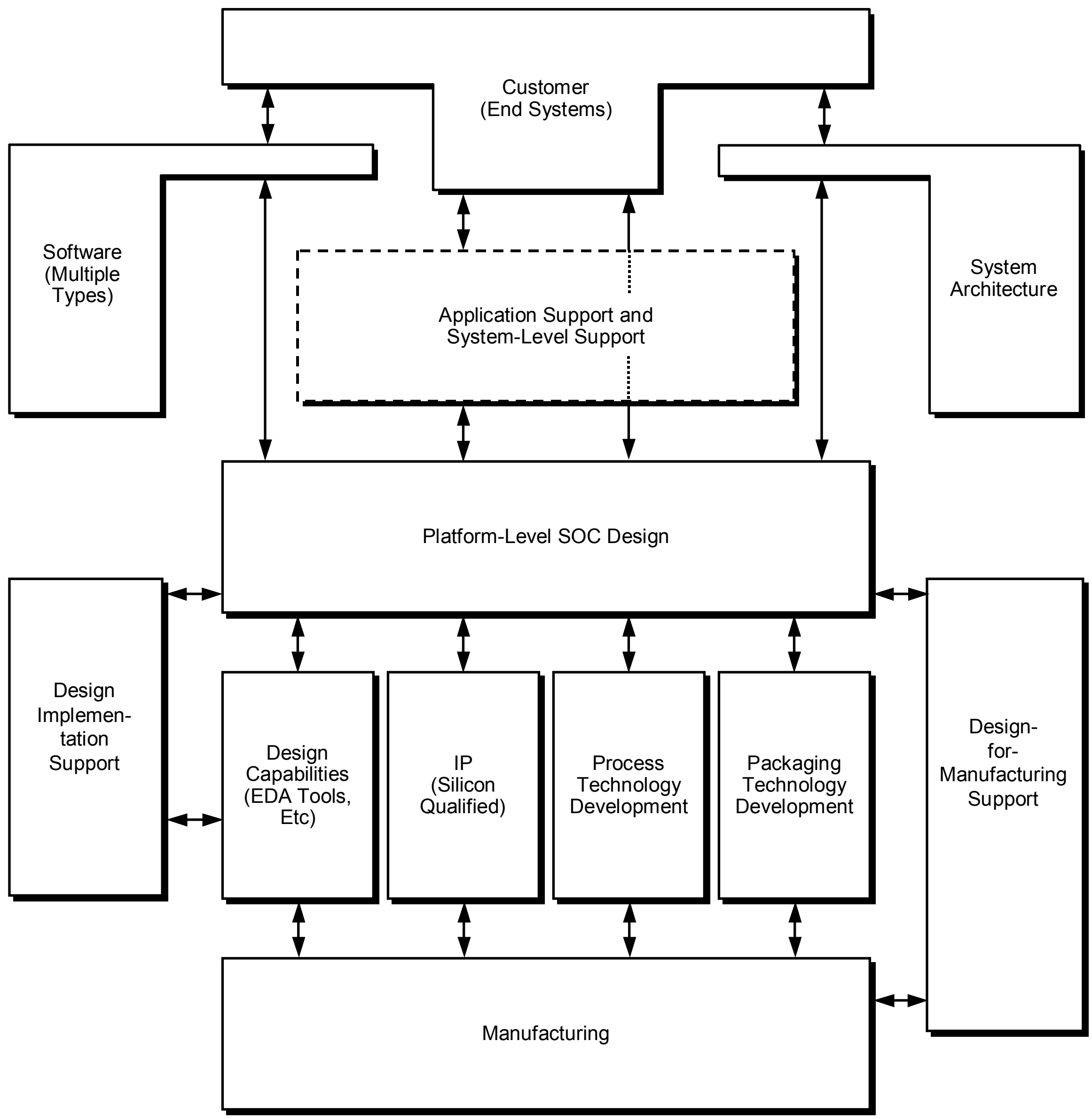
- The EDA industry needs to price based on value, which can increase market share as well as the total market. ***The IC industry needs to understand the value of EDA tools in order to provide larger budgets***.

  The value of design tools has not been established, and the EDA industry needs to change this.

It is critical to determine the factors for growth of the EDA market based on customer needs.

Hierarchy within the IC industry is shown in the following figure.

FIGURE 8
IC Industry Hierarchy



The issues regarding the hierarchy within the IC industry include:

- The design environment is evolving from being focused on IC chip designs to focusing on system designs, which means that the design skill base of IC vendors will need to increasingly address system-level architectural capabilities.

- Design implementation capabilities are depicted as a major discipline in the IC hierarchy. The reality is that design implementation capabilities become a key factor for effective participation in the IC market at 90nm.

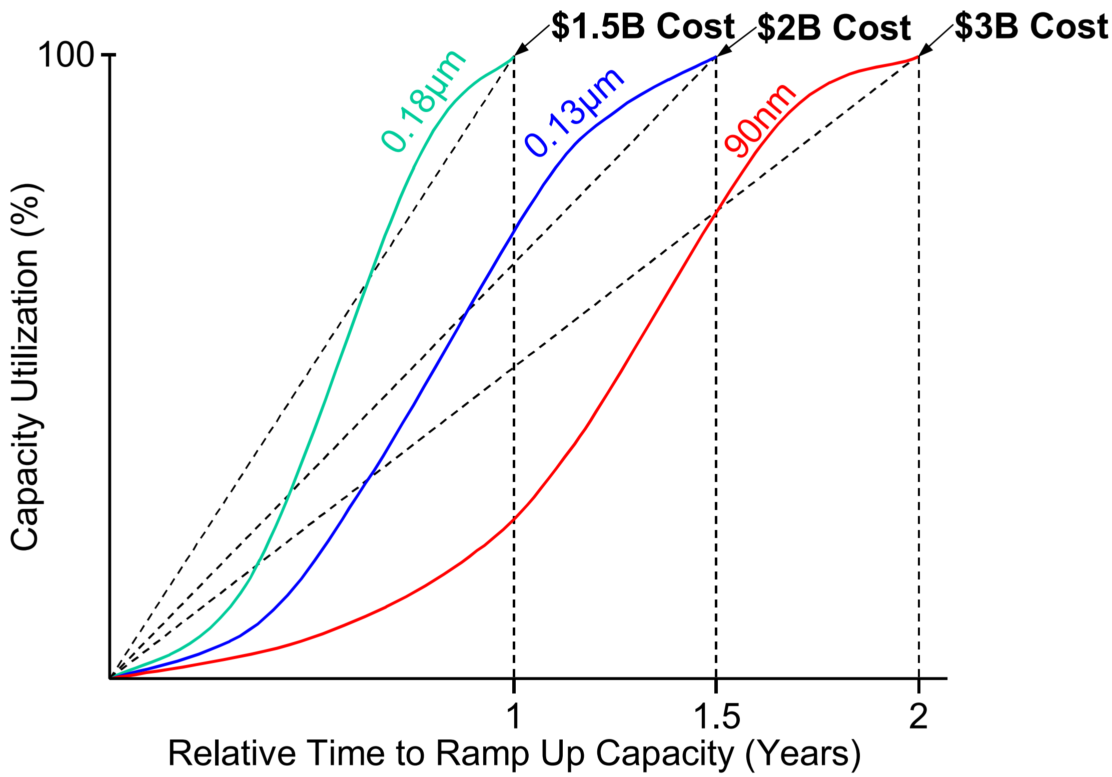
Areas of strategic capabilities within IC industry continue to evolve with the reduction in feature dimensions. It is important that IC vendors take a proactive approach to factors that will provide future success in IC business.

While IC vendors are generally concerned with relative positioning, they must also emphasize factors that will enable the overall IC market to generate growth longer term.

Design-for-manufacturability issues are becoming increasingly important for the IC industry as feature dimensions decrease. Design-for-manufacturability issues are resulting in lengthening the time required to ramp up new wafer fab facilities to high capacity utilization.

The ramp-up of wafer fab capacity utilization by feature dimension is shown in following figure.

FIGURE 9
Fab Ramp-Up Capacity Rate



The issues regarding fab capacity utilization ramp-up for logic products include:

- With a 0.18µm fab, annual depreciation costs (five year straight line) are $300M, and with a one-year ramp up, total absorbed costs are $300M.

- With a 90nm 300mm fab, annual depreciation costs (five year straight line) are $600M, and with a two-year ramp-up, total absorbed costs are $1.2B. While there can be the approach of staggering installation of equipment, etc, there are still large costs associated with ramping up 90nm 300mm facilities.

- High financial exposure associated with 90nm 300mm wafer fabs is resulting in a number of IDMs increasing use of foundry supply or installing facilities with a capacity of 10K wafers per month. The cost per wafer from a 10K per month wafer fab is higher than the cost per wafer of a 30K per month wafer fab (both fabs operating at high capacity utilization).

  The key issue is to establish powerful design implementation capabilities so that new products are developed within short time windows and so that wafer demand increases rapidly.

  There are very large cost savings from shortening the ramp-up schedule of 90nm wafer fab facilities from two years to one year, and it is important for the EDA industry to focus on addressing this opportunity.

  Leverage from powerful design implementation capabilities becomes very large at 90nm and even greater at 65nm. The EDA industry and design community have to focus on this leverage as opposed to on factors that were important in the past (cost of design tools, etc).

  EDA tool costs (generally 10 percent of total design project costs) are declining as a percentage of design project costs as feature dimensions shrink. The EDA industry needs to modify metrics so that they relate to benefits of a fast ramp-up of wafer fabs (significantly greater financial impact on IC vendors than cost of design tools). Shortening the time to ramp up a new fab facility at 90nm can have a financial impact of hundreds of millions of dollars for IC vendors.

The IC industry has traditionally used migration to smaller feature dimensions as the basis for enhancing functionality and reducing IC product costs.

The key metric for the rate of migration to smaller feature dimensions is the ramp-up in design completions at each new technology node (design completions considered to be more important metric than design starts).

Design completions by feature dimension are shown in the following table.

TABLE 7
Design Completions by Feature Dimension

	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007
>0.35µm	**7,410**	**5,997**	**3,517**	**1,852**	**1,085**	**647**	**396**	**347**	**302**	**217**	**143**	**92**	**47**
Growth rate (%)	NA	(19.1)	(41.4)	(47.3)	(41.4)	(40.4)	(38.8)	(12.4)	(13.0)	(28.1)	(34.1)	(35.7)	(48.9)
Percent total (%)	84.9	70.5	45.1	24.6	15.3	9.5	6.3	5.6	4.5	3.3	2.1	1.4	0.7
0.35µm	**1,187**	**2,138**	**3,421**	**3,841**	**2,508**	**1,841**	**1,254**	**697**	**502**	**346**	**271**	**172**	**101**
Growth rate (%)	NA	80.1	60.0	12.3	(34.7)	(26.6)	(31.9)	(44.4)	(28.0)	(31.1)	(21.7)	(36.5)	(41.3)
Percent total (%)	13.6	25.1	43.9	51.0	35.3	27.2	19.9	11.3	7.6	5.2	4.0	2.5	1.6
0.25µm	**126**	**372**	**811**	**1,582**	**2,797**	**3,186**	**2,871**	**2,276**	**1,643**	**801**	**643**	**464**	**178**
Growth rate (%)	NA	195.2	118.0	95.1	76.8	13.9	(9.9)	(20.7)	(27.8)	(51.2)	(19.7)	(27.8)	(61.6)
Percent total (%)	1.4	4.4	10.4	21.0	39.4	47.0	45.7	36.7	24.8	12.1	9.5	6.9	2.8
0.18µm	**0**	**0**	**47**	**251**	**672**	**985**	**1,295**	**1,946**	**2,705**	**2,864**	**2,378**	**1,791**	**1,104**
Growth rate (%)	NA	NA	NA	434.0	167.7	46.6	31.5	50.3	39.0	5.9	(17.0)	(24.7)	(38.4)
Percent total (%)	0.0	0.0	0.6	3.3	9.5	14.5	20.6	31.4	40.8	43.4	35.2	26.5	17.1
0.15µm	**0**	**0**	**0**	**0**	**33**	**105**	**346**	**591**	**874**	**1,193**	**1,576**	**1,837**	**1,641**
Growth rate (%)	NA	NA	NA	NA	NA	218.2	229.5	70.8	47.9	36.5	32.1	16.6	(10.7)
Percent total (%)	0.0	0.0	0.0	0.0	0.5	1.5	5.5	9.5	13.2	18.1	23.3	27.2	25.5
0.13µm	**0**	**0**	**0**	**0**	**0**	**14**	**127**	**327**	**561**	**978**	**1,371**	**1,804**	**2,478**
Growth rate (%)	NA	NA	NA	NA	NA	NA	807.1	157.5	71.6	74.3	40.2	31.6	37.4
Percent total (%)	0.0	0.0	0.0	0.0	0.0	0.2	2.0	5.3	8.5	14.8	20.3	26.7	38.4
90nm	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**11**	**51**	**194**	**372**	**561**	**792**
Growth rate (%)	NA	NA	NA	NA	NA	NA	NA	NA	363.6	280.4	91.8	50.8	41.2
Percent total (%)	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.2	0.8	2.9	5.5	8.3	12.3
<90nm	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**4**	**39**	**105**
Growth rate (%)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	875.0	169.2
Percent total (%)	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.1	0.6	1.6
TOTAL Designs	**8,723**	**8,507**	**7,796**	**7,526**	**7,095**	**6,778**	**6,289**	**6,195**	**6,638**	**6,593**	**6,758**	**6,760**	**6,446**
Growth rate (%)	NA	(2.5)	(8.4)	(3.5)	(5.7)	(4.5)	(7.2)	(1.5)	7.2	(0.7)	2.5	0.03	(4.6)

The ramp-up of 90nm and sub-90nm designs is slow due to difficulties in implementing designs and high design costs. Also, the probability of designs operating as expected in systems declines as complexity increases.

Revenue per designs at 90nm will need to be high in order to cover the impact of high design costs. However, it is critical that designs are completed within the expected time windows in order to avoid large price reductions associated with being late to market.

Design completions are closely linked with the changing cost metrics of the IC industry and the increasing importance of ensuring first-time success with IC designs in silicon.

The cost of implementing IC designs is increasing with the reduction in feature dimensions, which is shown in following figures.

FIGURE 10a
Cost of Implementing Designs

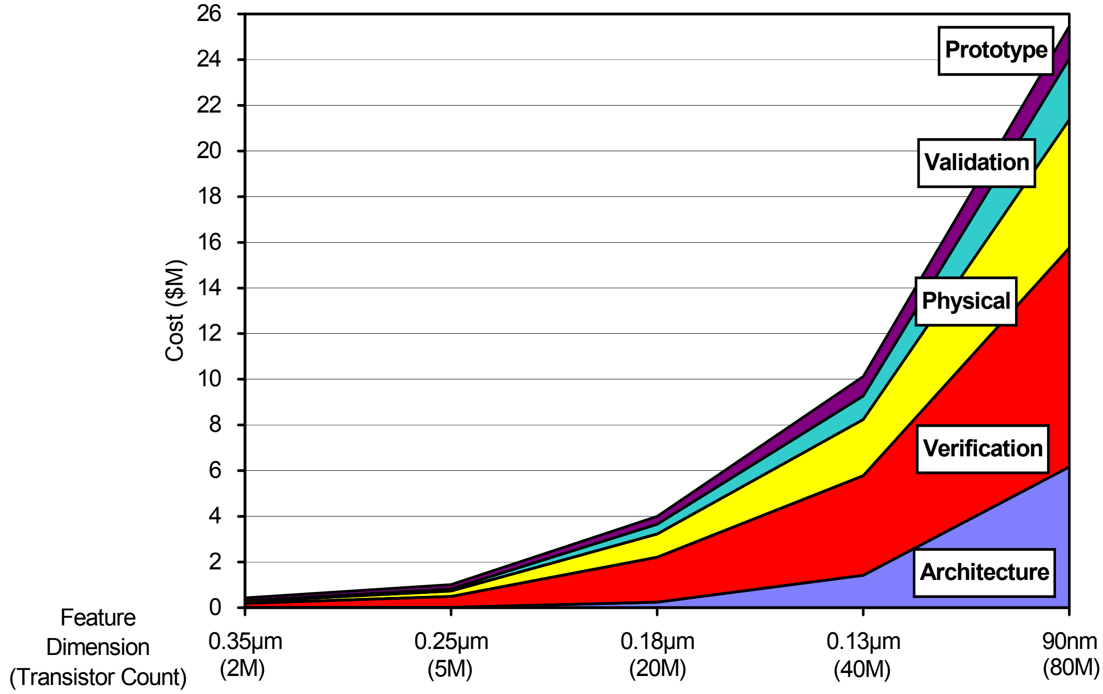
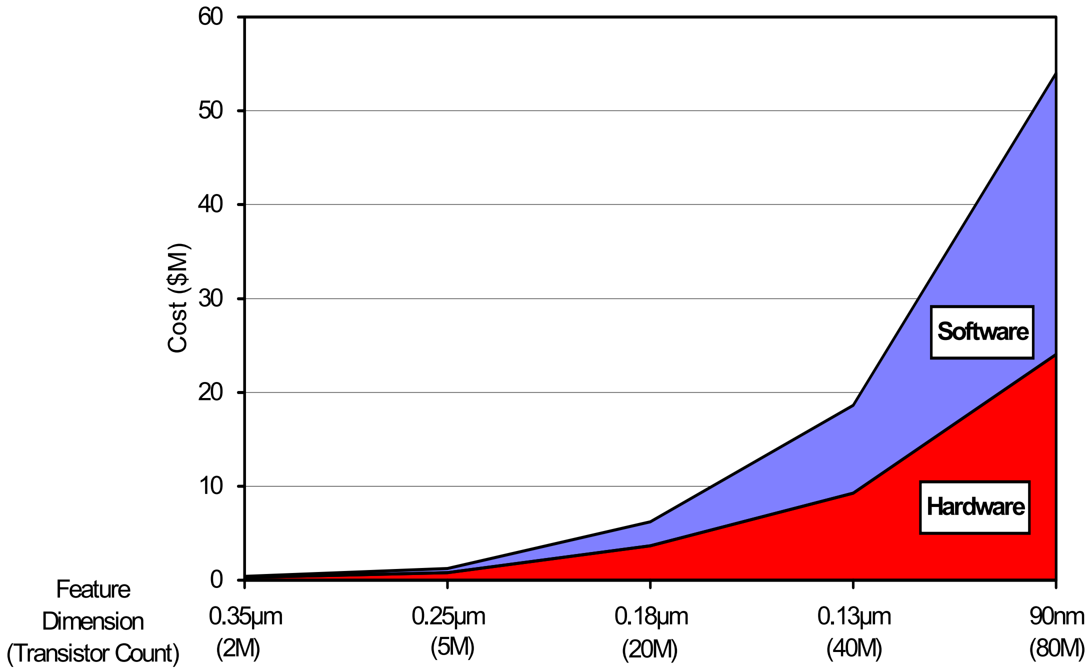


FIGURE 10b
Cost of Implementing Designs



The issues regarding design implementation costs include:

- The increase in cost per design (based on case studies) is related to the increasing design complexity (90nm designs at 80M transistors versus 0.13μm designs at 40M transistors) and the expansion of databases that have to be managed due to lower operating voltages, etc.

- Design implementation costs include the architecture component, which is evolving from system level to IC level. As IC designs become platform-level solutions, system architecture can migrate completely to the IC design arena.

- Validation costs relate to the operation of IC within the end system. ICs must operate effectively within the range of system operating environments, which can involve extensive evaluation.

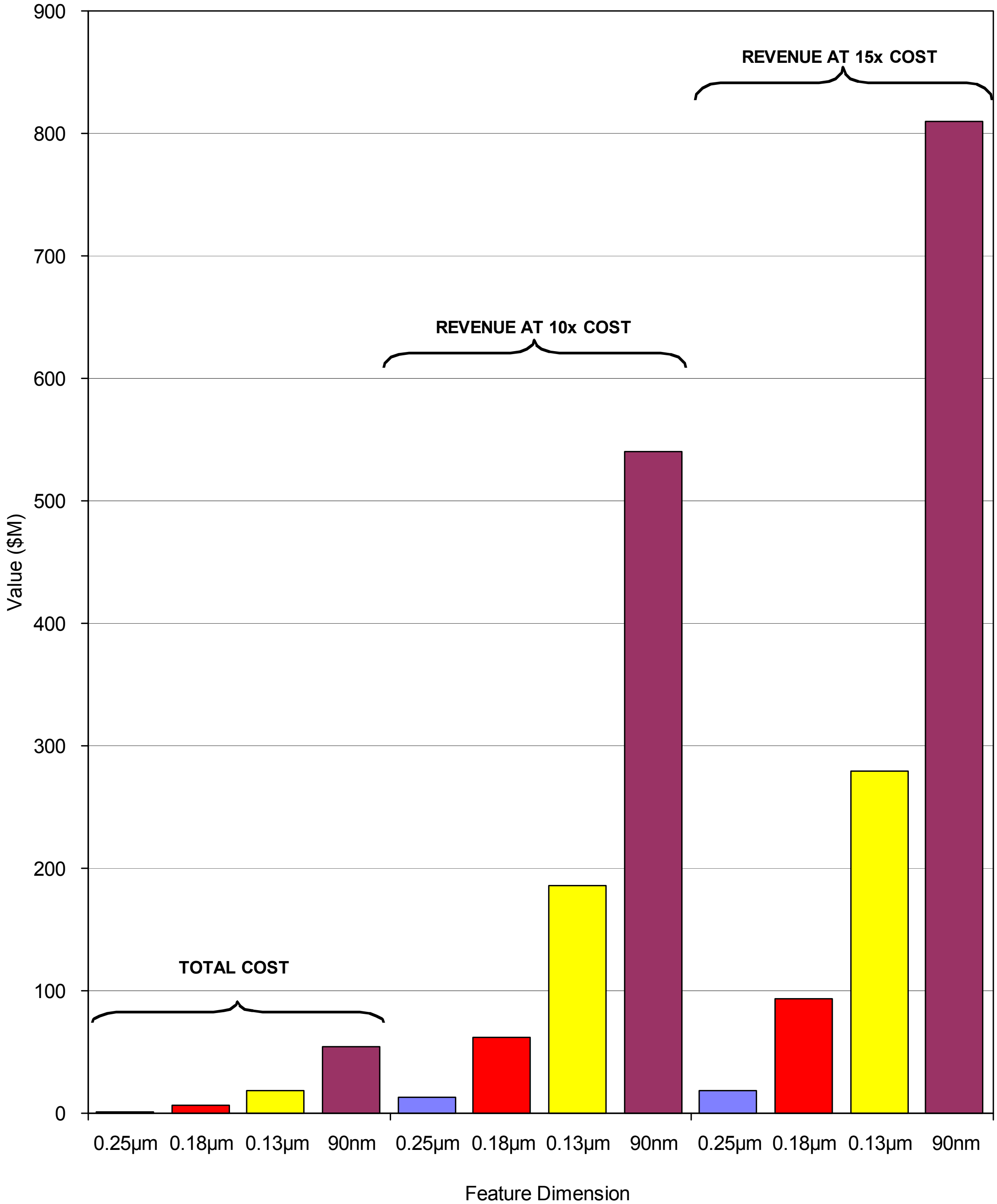
- Prototype costs include the cost of reticles and wafer lots. Reticle costs are increasing with the reduction in feature dimensions ($1.2M to $1.5M at 90nm) but represent a relatively small percentage of total design costs (less than 10 percent).

- The cost of software development is increasing rapidly, and for many designs, the cost of software development can exceed the cost of hardware development.

The increasing costs of IC designs require higher revenue per design in order to obtain good payback.

A perspective on revenue per design is shown in the following figure.

FIGURE 11
Revenue Per Design



The issues regarding revenue per design include the following:

- Revenue per design is shown for 10x and 15x design implementation costs.

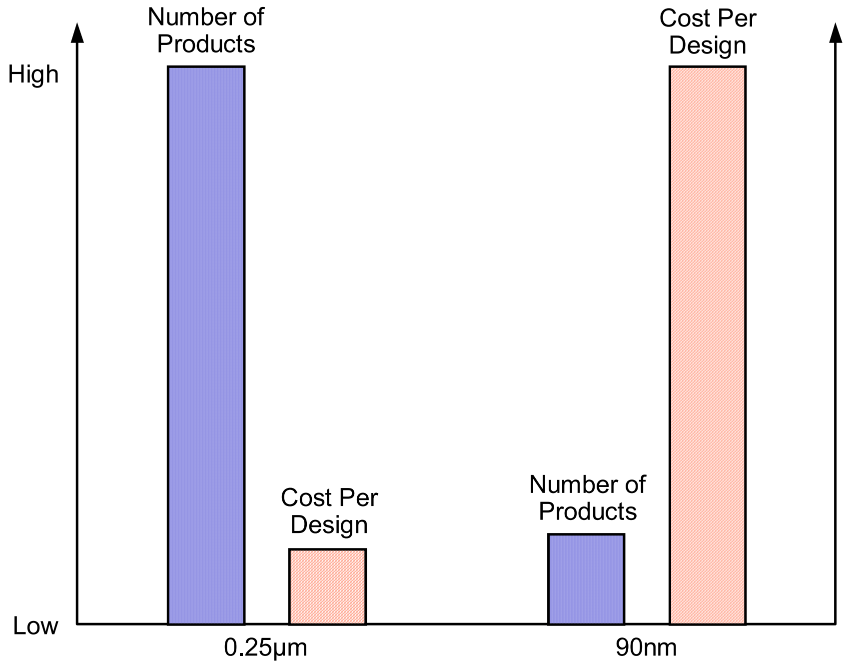
  Values are shown for designs with selected feature dimensions.

- Revenue required per design to give reasonable payback shows high growth with a reduction in feature dimensions, which indicates importance of completing designs within required windows and ensuring that revenues are optimized from the market.

Design capabilities become key factors in revenue leverage of the IC industry because of increasing costs and the strategic importance of product positioning leadership.

A perspective on the IC design environment at 90nm and 0.25μm is shown in the following figure.

FIGURE 12
Design Issues at 0.25µm and 90nm



Many designs are implemented at 0.25µm, and the cost per design must be low. At 90nm, few designs will be implemented, and the cost per design will be high. There are high technical and financial risks associated with 90nm designs.

Efficiency in design implementation represents the key factor that bridges 0.25µm and 90nm environments.

Market and financial risks associated with the 90nm technology node are evident. Reducing design implementation costs through structured ASICs, software programmability, highly complex FPGAs, etc, has benefits; however, there must also be 10x increased design productivity for each new technology node if the IC industry is to have high revenue growth longer term.

The costs of bringing up new generations of process technology and implementing new designs are increasing. Payback metrics for the IC industry will need to change.

The EDA industry and design community need to become much more closely coupled to financial metrics within the IC industry than in past.

The analysis of design project case studies includes:

- Case studies at 0.13µm have been analyzed to understand the composition of design teams, design completion costs, design complexity, and difficulty levels of designs, which are based on performance, etc. Difficulty levels of design involve an in-depth analysis of design characteristics as well as time-to-market pressures.

- IC designs within different IC vendors were analyzed, with visibility into the importance of design implementation leadership to top management. Assessment of design implementation capabilities correspond to inputs from customers.

The case studies are for designs at 0.13µm because wafer process technology is relatively mature and because several companies have successfully implemented designs at this technology node.

The summary of data on case studies is shown in following table.

TABLE 8
Design Cost Effectiveness (0.13μm) (Complexity Versus Cost)

Company	Gate count	Difficulty	Design complexity	Completion cost ($M)	**Ratio of complexity/cost (high is best)**	Completion time (months)	**Ratio of complexity/time (high is best)**	**Importance of design expertise***
A	10.5	7.2	75.6	9.84	**7.68**	11.64	**6.49**	**8**
B	7.6	6.3	47.9	9.87	**4.85**	12.45	**3.85**	**4**
C	12.4	6.6	81.8	11.36	**7.20**	9.41	**8.70**	**7**
D	5.8	4.5	26.1	6.31	**4.14**	11.18	**2.33**	**3**
E	6.9	5.6	38.6	6.92	**5.58**	11.86	**3.26**	**5**
F	8.7	8.2	71.3	9.43	**7.57**	12.64	**5.64**	**7**
G	8.6	7.5	64.5	7.81	**8.26**	10.15	**6.35**	**8**
H	13.1	6.7	87.8	10.92	**8.04**	12.46	**7.04**	**8**

* Note:
Customer inputs.

The analysis of designs includes:

- The gate count levels of designs at 0.13μm range from 5.8M up to 12.4M. Designs with high logic content were selected.

- The difficulty factor involves performance requirements of designs, integration of demanding functions such as high-speed interfaces, need for low power, need for chip area minimization, etc.

  The difficulty factor also involves subjective factors but provides visibility into the challenges for IC vendors. It is important to account for the difference in complexity levels of design projects.

- The design complexity is a multiple of gate count and difficulty.

- The design completion costs cover costs from specification generation through tested prototypes and are based on number of engineers, time spent by engineers on projects, and loaded cost of engineers.

- Ratio of complexity to cost provides perspective on relative competitiveness of IC vendors in implementing designs. The range of IC capabilities (4.14 to 8.26) can impact the competitiveness of IC vendors in the future.

- Completion times are shown in months, but completion times for all designs were in relatively narrow windows (selection process to eliminate designs that were simple iterations of previous designs).

- The ratio of complexity to time is an indicator of competitiveness of IC vendors in terms of fast time-to-market for new designs. Values range from 2.33 to 8.70, which shows significant variation in the ability of IC vendors to bring new designs to market within short time windows.

- The analysis of case studies indicates that there is direct correlation between complexity and cost and between complexity and time-to-completion, ie, IC vendors that have the best design capabilities are lowest-cost and bring their new products to market fastest (thereby obtaining price premiums for their products).

  Although the data is for a small number of designs only, the pattern is consistent across most designs within selected IC companies.

- There is also a correlation between customer assessment of capabilities of selected IC vendors and performance of IC vendors in design implementation based on metrics shown.

The analysis of design implementation capabilities of IC vendors provides a basis for determining profitability and market positioning in future, which will directly

relate to market valuation. Shareholder value in the future will be directly related to emphasis placed on design implementation capabilities short term.

The emphasis by IC vendors on design implementation leadership can have major payback to shareholders and should be the metric to project future competitive positioning of IC vendors.

While it is important to have access to appropriate wafer fab capabilities, without access to leadership design implementation capabilities, IC vendors will not be financially successful in future.

The key issues in the design arena include:

- IC design costs account for 10 to 15 percent of IC revenues but will increase to 20 percent of revenues in the future.

  EDA tool costs account for 10 percent of design costs, ie, 1.0 to 1.5 percent of IC revenues.

  IC revenues account for 10 to 20 percent of equipment revenues.

  EDA tool costs account for 0.1 to 0.2 percent of equipment revenues.

  The key challenge for the EDA industry is to increase EDA expenditures as a percentage of revenues for IC and equipment markets. The EDA industry needs to relay benefits to customers, ie, to the IC industry (financial metrics).

  The key challenge for the IC industry is to make more effective use of EDA tools and quantify benefits of design tools.

- Design tool budgets are based on the past expenditures of IC vendors, and the allocation of R&D expenditures is based on planned projects.

  EDA budgets are managed by CAD organizations of IC vendors, with minimal flexibility in expanding budgets.

  EDA budgets should be based on benefits to IC vendors, which involves increased productivity of design engineers, higher IC revenues and profits, and larger market capitalization of IC vendors. Decision processes must be elevated to top-level managers within the IC industry.

- The structure of the IC design environment must change in order to increase EDA TAM. The key requirement is to quantify the value of the EDA industry to the IC industry.

- The IC market is in a recovery mode, with the expectation of growth in 2004 and 2005. It is likely that 2006 will be a down year for the IC industry.

  The EDA market should be in a growth position short term because of the recovery of the IC market, but high growth longer term will depend on changes in relationships with IC vendors.

- R&D expenditures will increase, which could lead to higher EDA expenditures if customers understand the value of design capabilities.

- EDA tool licenses represent approximately 1.0 percent of many IC vendors' revenues. Significant upside potential exists in the growth of the EDA market if the value of EDA tools is demonstrated.

- The EDA industry continues to develop new tools. The key issues are how to help customers be successful from these technology capabilities and demonstrating financial benefits of using new EDA tools.

  Although the EDA industry has traditionally focused on technology metrics, it is important to add financial metrics that allow additional revenue streams to be addressed.

- The competitive position of IC vendors is increasingly tied to the effective use of EDA tools. Gross margins and market valuations are directly tied to design capabilities.

  The EDA industry needs to proactively drive the benefits of better tools and financial benefits for IC vendors in more effective use of design tools.

The EDA industry has very high growth potential if financial benefits of leadership design implementation capabilities are understood by IC and electronics industries, ie, customers.